Fourth Order Butterworth Gm-C Lowpass Filter in 0.18u CMOS

John Warwar

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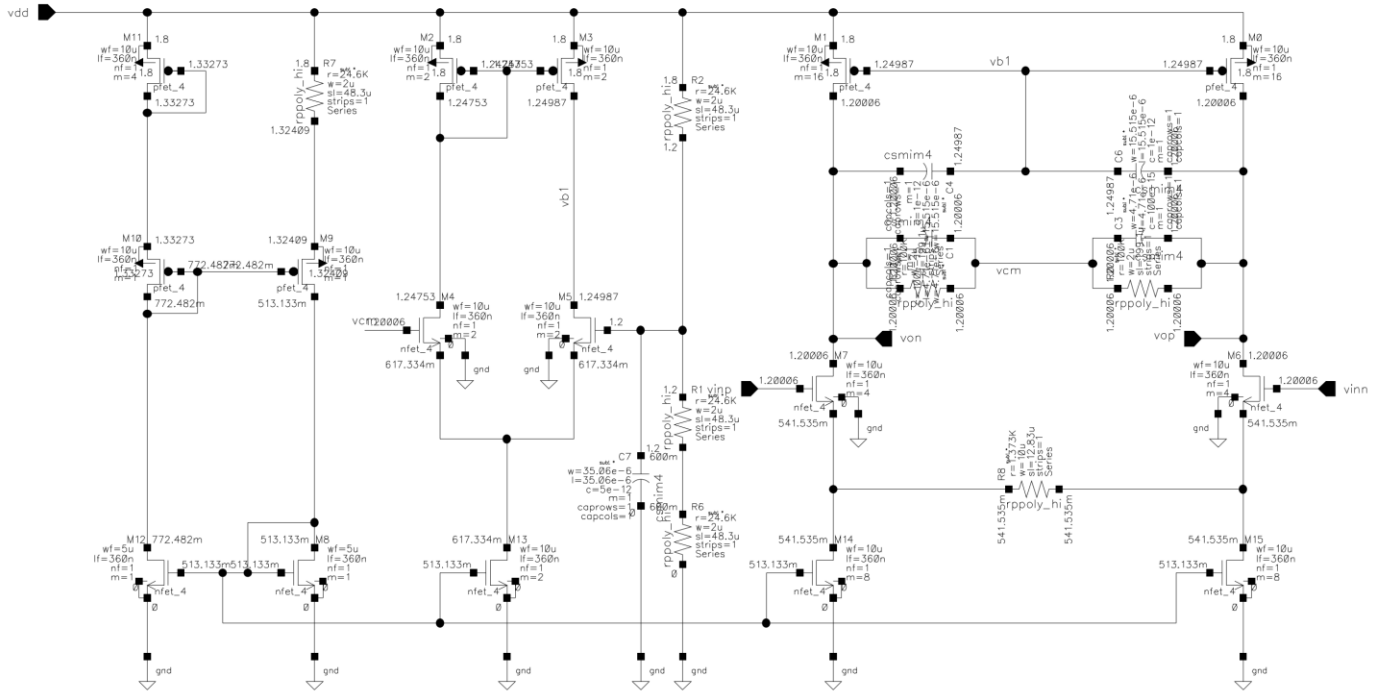
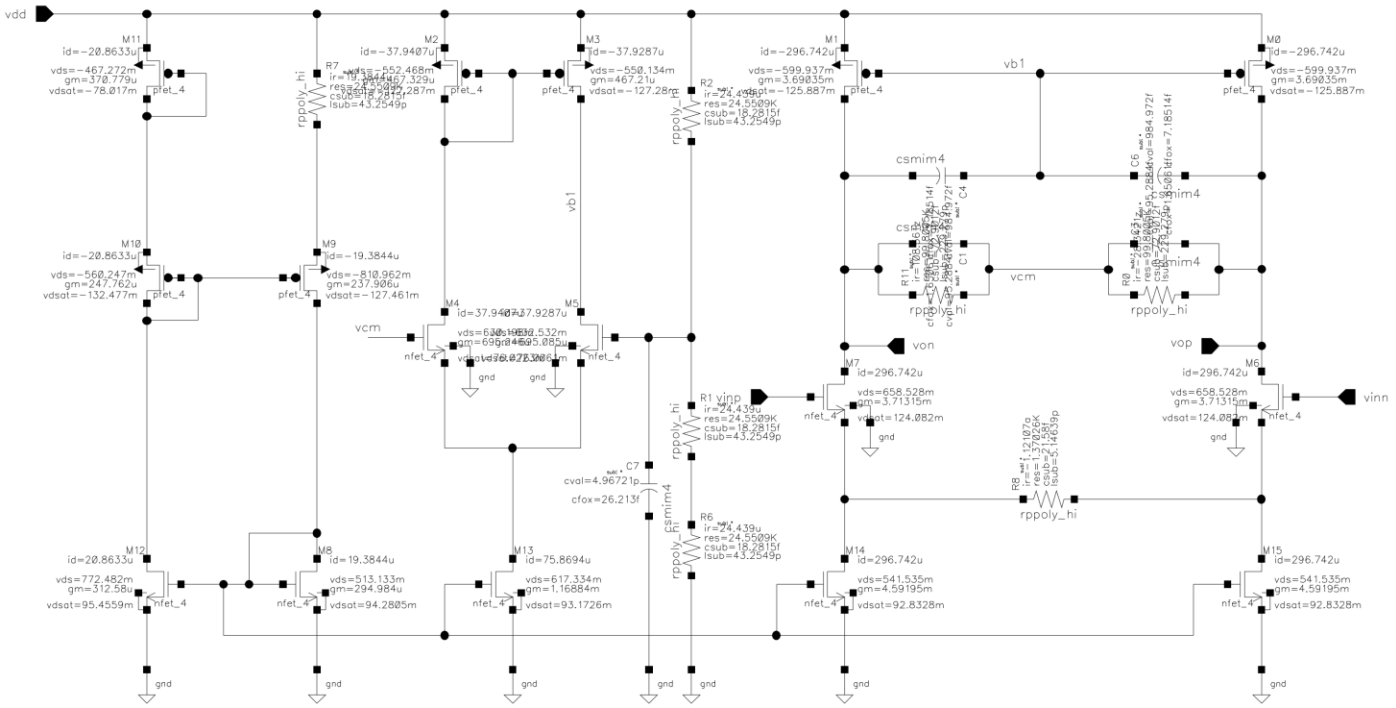
Professor Hossein Hashemi

Achieved Performance

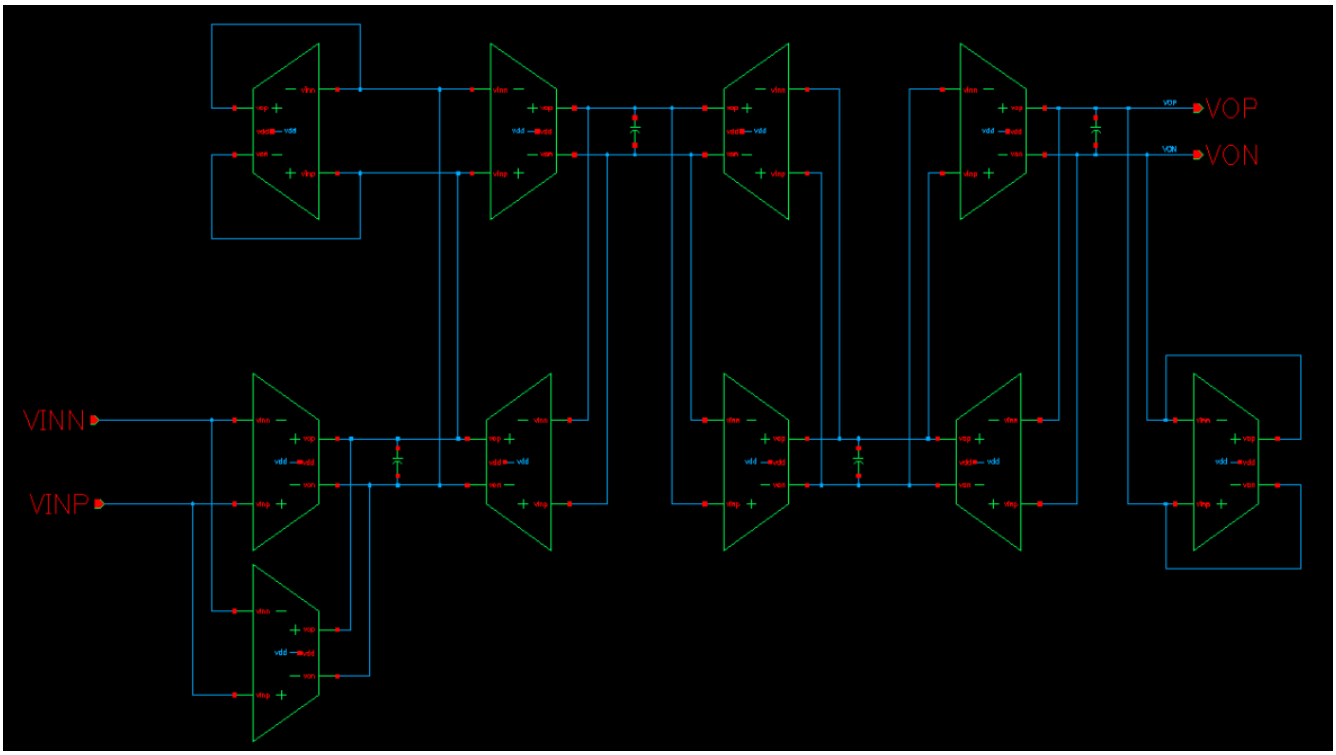
Specification	Desired	Achieved	Analytical Estimate
Filter -3dB cutoff frequency	1 MHz	996.3 kHz	1 MHz
Passband gain	0 dB	0.157 dB	0 dB
Input-referred noise power spectral density	< 25 nV/sqrt (Hz)	26.6 nV/sqrt(Hz) @ 1/f corner	19.125 nV/sqrt (Hz)
Total harmonic distortion @ Vin,pp = 1V	< 1%	5.1%	-
Total current consumption	< 10 mA	7.3 mA	-
Temperature range	-25°C to 85°C	-25°C to 85°C	-
Supply Voltage Range	1.7 V to 1.9 V	1.7 V to 1.9 V	-

Component Parameters and DC Operating Points

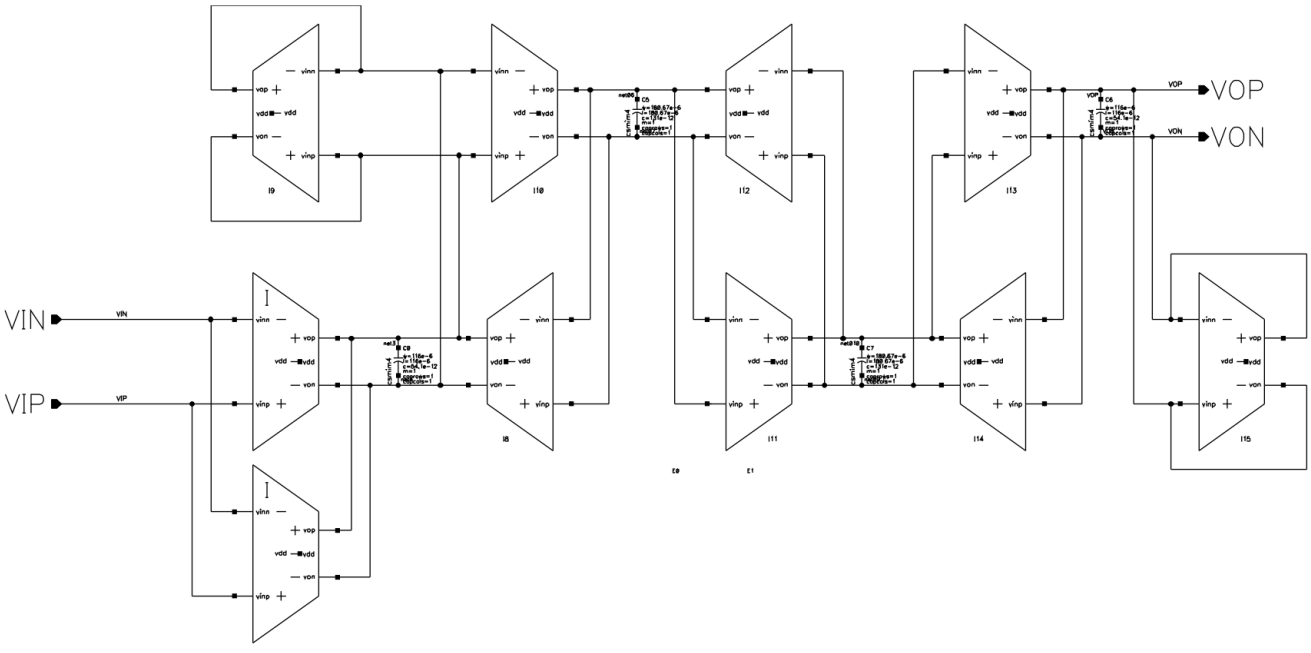




Top Level Filter Structure



Schematic with Capacitance Values



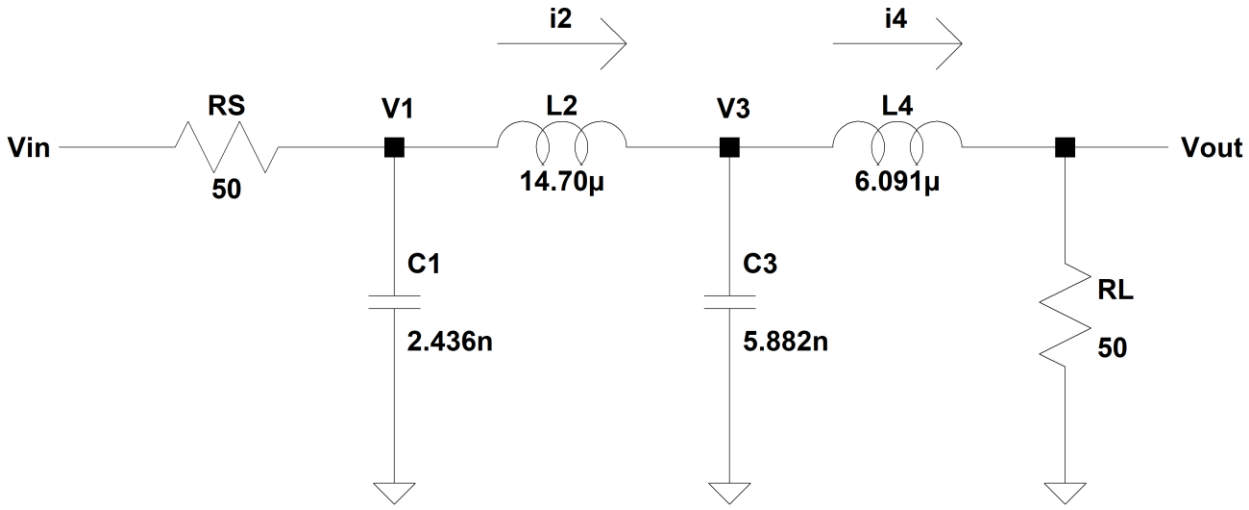
Design Strategy and Analytical Calculations

Determining the Topology

A low-pass fourth order Butterworth filter has a frequency normalized transfer function of

$$H(s) = \frac{1}{s^4 + 2.6131259s^3 + 3.4142136s^3 + 2.6131259s + 1}$$

This butterworth filter can be implemented in many different ways. One way to realize this filter is with the passive network structure seen in the figure below. I used this passive ladder filter as the basis for my active structure.



Ladder filters are generally considered to be less sensitive to exact component values than other structures such as cascades of biquads, which seemed appealing since component tolerances as well as nonideal parasitics can lead to uncertainties in exact filter parameters in an integrated circuit implementation. It should also be noted that this passive filter has an attenuation of 6dB at DC which I compensated for in my active filter implementation of this structure. Using KCL and KVL, the nodal equations describing this filter can be found. Each equation can be arranged as an integrator. This allows the creation of a signal flow diagram based on four integrators. This in turn can be mapped into Gm-C active filter implementation of this system.

$$\frac{V_1 - V_X}{R_s} + V_1 sC_1 + i_2 = 0 \qquad \rightarrow \qquad V_1 = \frac{\frac{V_X - V_1}{R_s} - i_2}{sC_1}$$

$$i_2 + V_3 sC_3 + i_4 = 0 \qquad \rightarrow \qquad V_3 = \frac{i_2 - i_4}{sC_3}$$

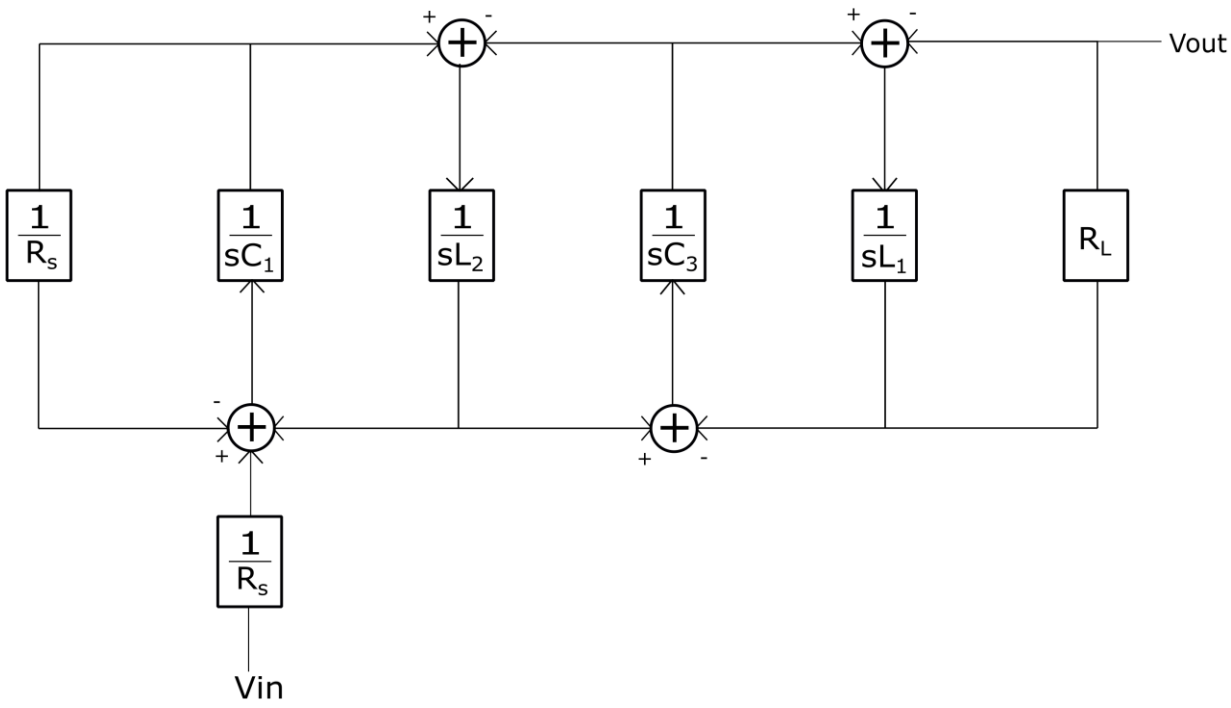
$$i_2 = \frac{V_1 - V_3}{sL_2}$$

$$i_4 = \frac{V_3 - V_Y}{sL_4}$$

$$-i_4 + \frac{V_y}{R_L = 0} \qquad \rightarrow \qquad V_Y = i_4 R_L$$

Component Scaling

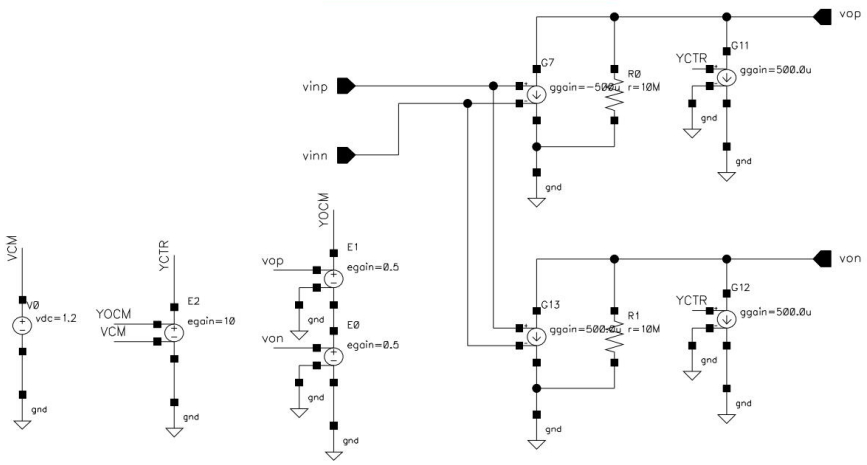
In the passive network shown above, the size of the components would make it practically impossible to implement into a real integrated circuit. Therefore, many of the nodes within the system need to be scaled appropriately to yield reasonable and obtainable component values. After finding the passive circuit structure and performing the nodal analysis, the signal flow diagram seen below was derived.



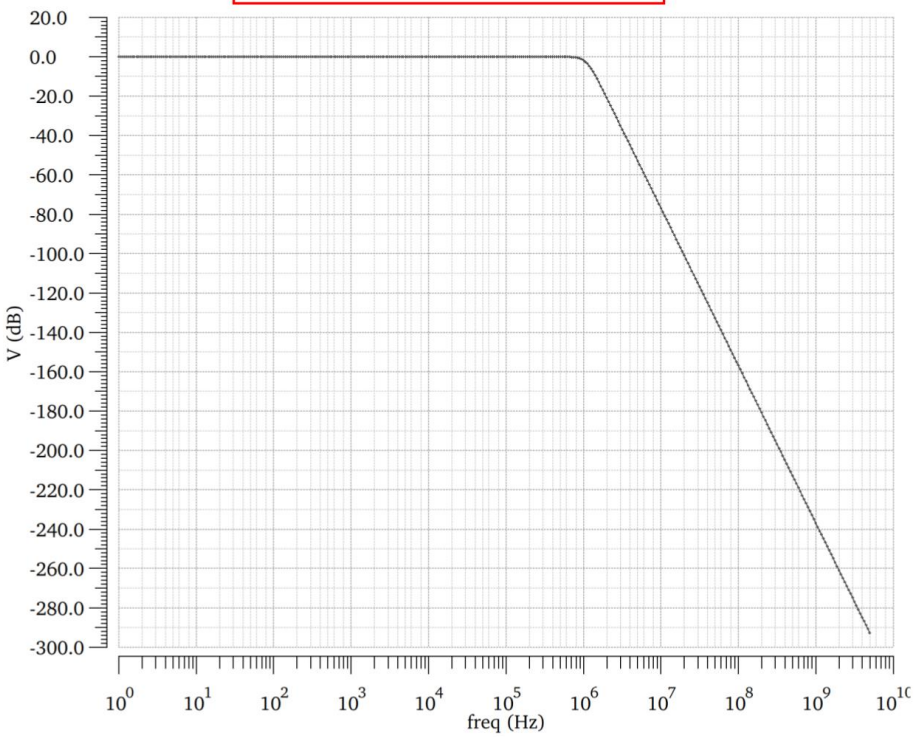
Ideal Simulation of Structure

After determining that the filter topology I chose was consistent with the transfer function and filter specification, I built and ideal model of the implementation in Cadence. This was accomplished through the use of ideal voltage-controlled-current-sources and voltage-controlled-voltage sources, as seen in the figure below.

Ideal OTA Schematic

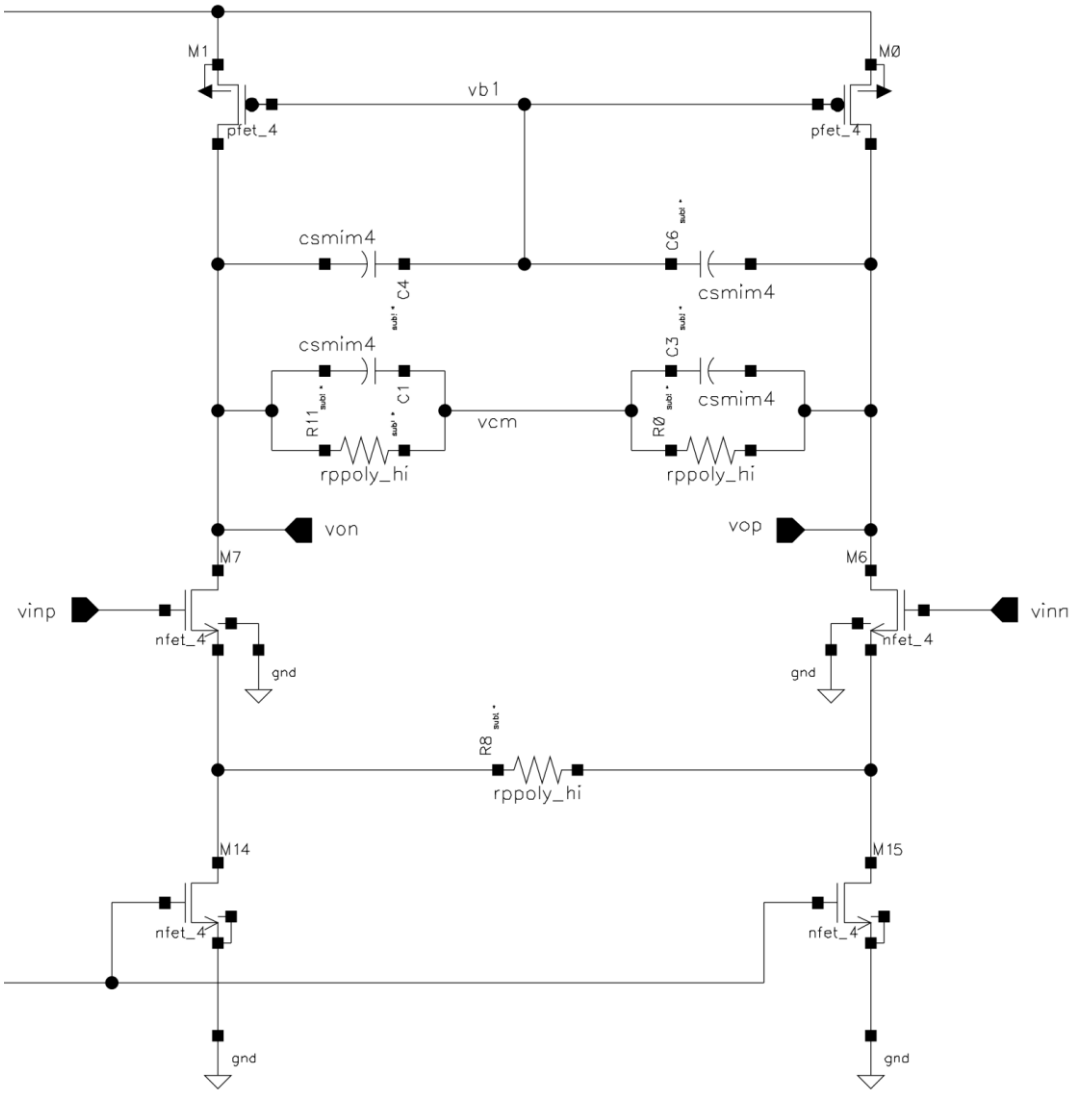


Ideal OTA Magnitude Response



Designing a Linear Gm-Cell

There are various topologies that can achieve highly linear operational transconductance amplifiers. Multiple topologies were designed and tested for the Gm transconductor building block. However, headroom issues severely limited most of the designs that were tried, and I ended up using a relatively straightforward transconductance stage with the resistive degeneration and split tail current sources. This yielded the most headroom, but it was still challenging to achieve 1 Vpp operation. All transistors were sized and biased to remain in the saturation region and the input devices were as large as possible so that the Gm of the cell would be primarily determined by the degeneration resistor. The structure of the Gm-cell can be seen in the schematic below.

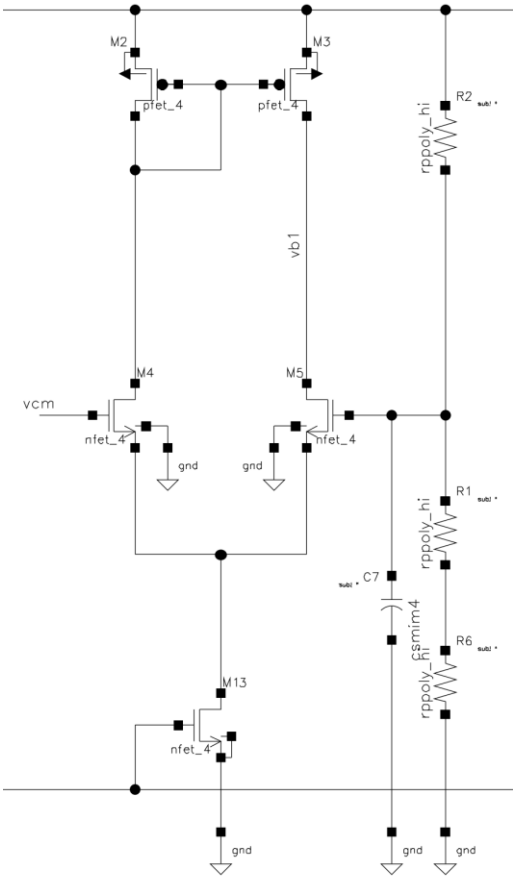


The transconductor itself was designed to target a transconductance value of Gm = 5e-4. The filter structure was scaled so that one transconductor stage could be used throughout the whole

design. The passive components provided the additional degrees of freedom to match the filter function. The value of 2k was also chosen based on the total allowed power of the filter and the desired voltage dynamic range. In particular, with a 0.5V amplitude input, a transconductance value of 5e-4 results in about 300uA of current at the output nodes of the transconductor. This seemed consistent with a transconductor biased at about 640uA which would lead to an overall acceptable power consumption given the budget of 10mA.

It should also be noted that the transconductor at the input of the filter was doubled to account for the attenuation of 2 by the DC attenuation of the passive filter upon which my design was based. Additionally, when this cell is implemented into the full filter structure, the two capacitors connected between the output nodes change the Gm-C relationship and must be accounted for when sizing the external capacitors.

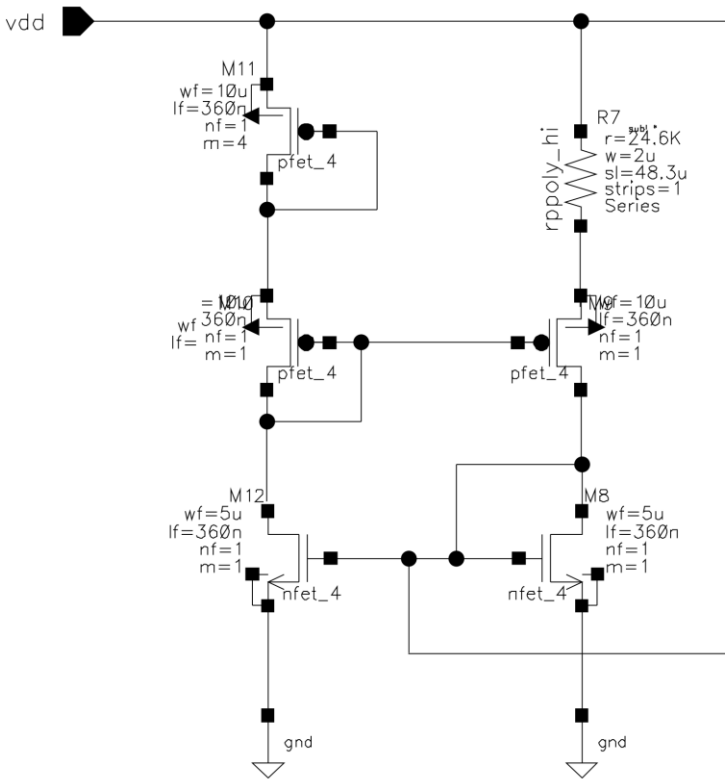
Common Mode Feedback



I designed a high gain common mode feedback loop which could precisiely set the common mode to the optimum value such that all the devices would have the most headroom. The common mode feedback appeared to be stable when analyzed as a single treansconductor stage. Specifically, the internal common mode feedback path was stable assuming the common mode input bias was driven by an independent source. A second common mode feedback loop exists

however when multiple trasnconductor stages are connected in a feedback loop. I discovered this during the transient simulations and was able to stabilize this second common mode feedback path with my high gain CMFB loop by scaling down the sizes of devices as well as adding capacitors across the output nodes, with the common mode connected between them. This seemed to completely fix the stability issues and provided ample phase margin and gain margin, which will be discussed in a later section.

PVT Insensitive Biasing Scheme

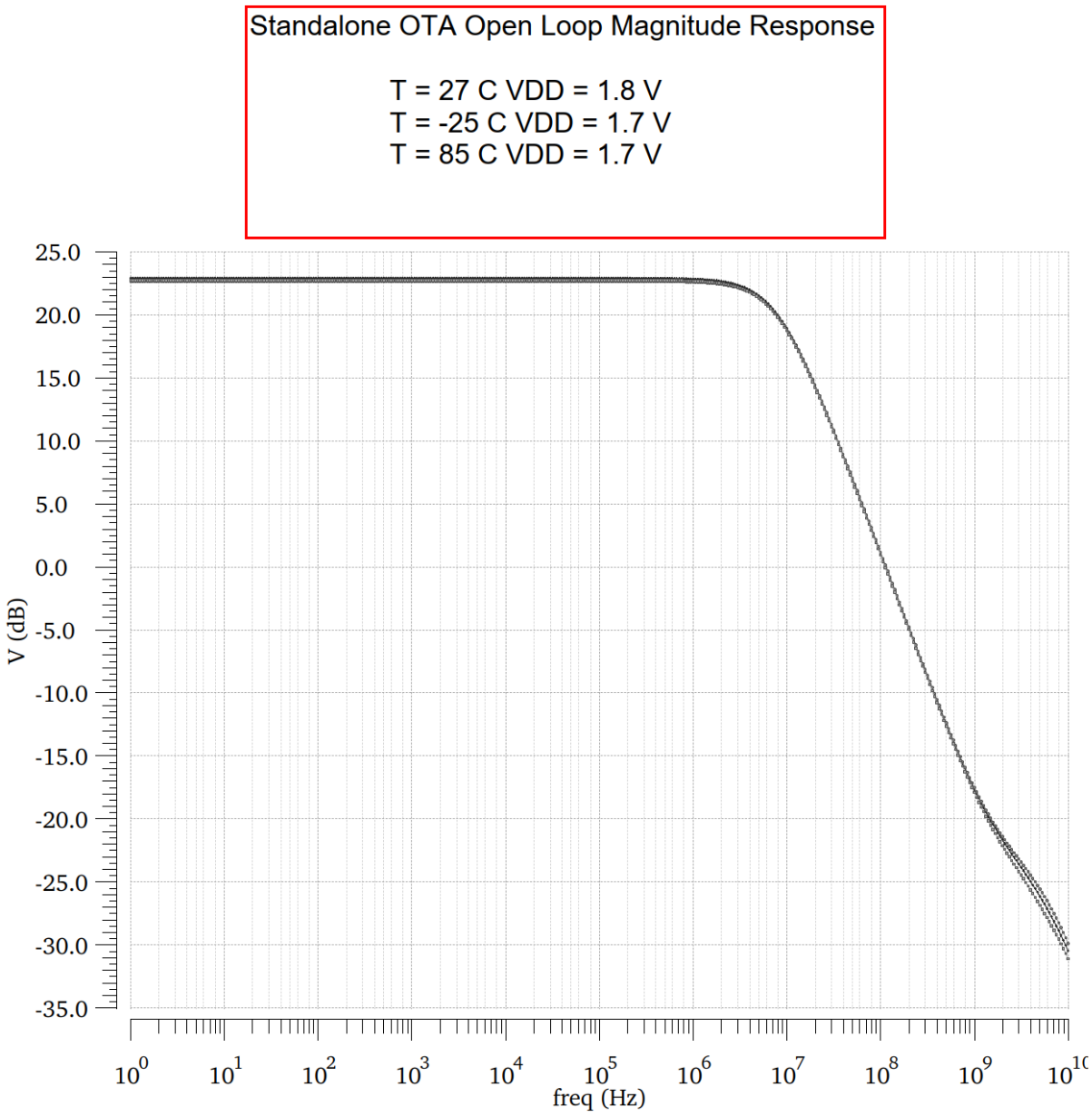


The supply independent bias circuitry seen above was used as the basis for the biasing scheme in the Gm-cell. The lengths of the devices in these branches were chosen to be sufficiently larger than the minimum length to reduce undesirable effects like channel length modulation. This structure is typically designed upside down with the resistor hooked from the lower NFET to ground and the reference voltage tapped off of the PMOS devices. However, this scheme was more conducive to my design used since I was using NFETS as the current sources in the CMFB and linear Gm circuitry.

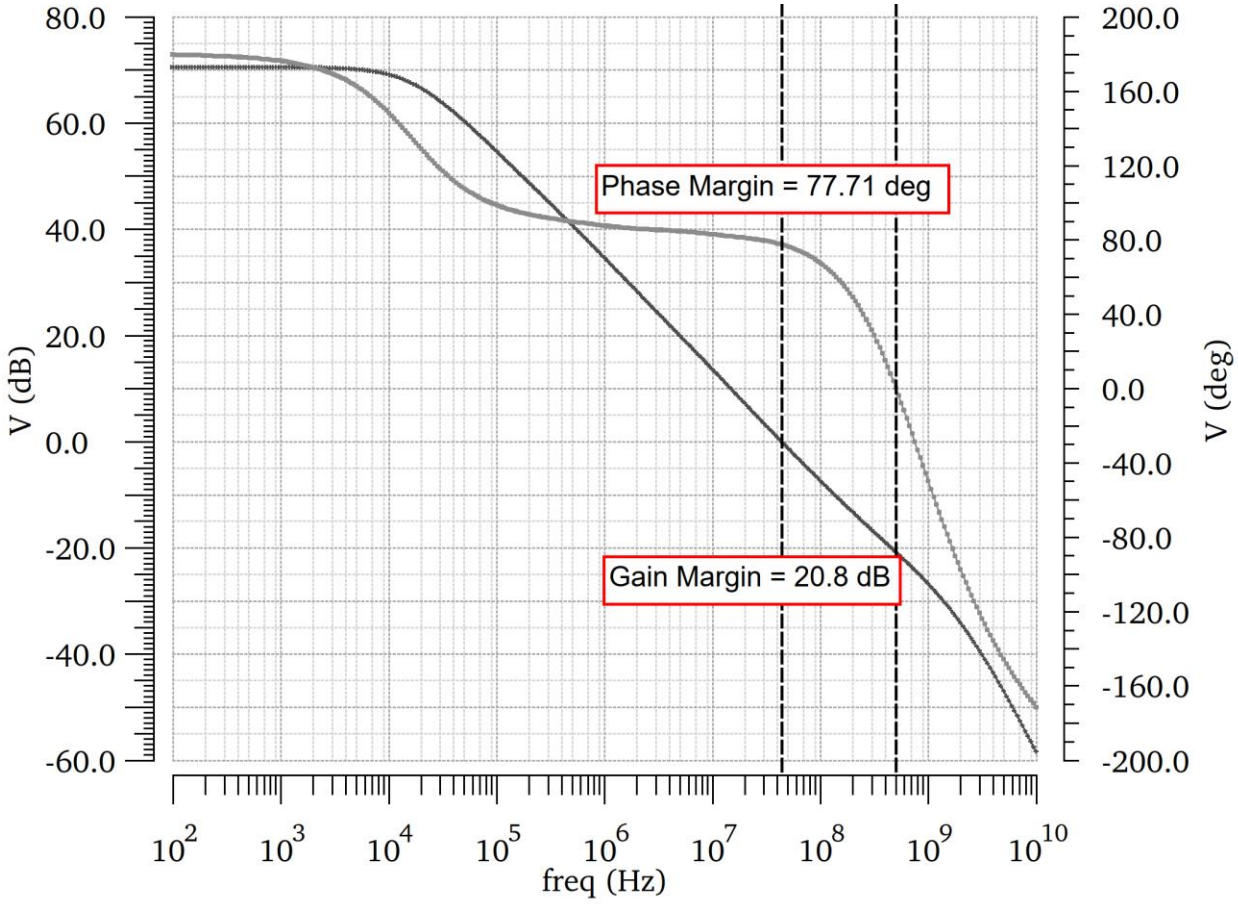
Power

After determining the top-level filter structure and performing the ideal simulation to ensure proper functionality, I determined what the biasing and power consumption of the various blocks of the circuits would be. Since the structure requires 10 of the linear Gm-cells, and the power budget was set to a current limit of 10 mA, the power consumption of each cell could not surpass 1 mA to meet the requirement. With this allotted budget, I chose to spend the most current in the actual Gm-cell differential pair with the resistive degeneration and split tail current sources. By burning more current in these branches, the noise was effectively lowered since nearly all the noise, as seen in the noise summary, came from the devices in these branches. Overall, about 80% of the current was burned through these branches, with the other 20% going through the common mode feedback circuitry as well as the PVT bias circuitry. In the end only 7.3 mA out of the 10 mA was used, so further revisions in the design could very likely lower the noise to well below the desired value of 25nV/sqrt (Hz).

Results


Standalone OTA Open Loop Magnitude Response
T = 27 C VDD = 1.8 V
T = -25 C VDD = 1.7 V
T = 85 C VDD = 1.7 V
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
-10.0
-15.0
-20.0
-25.0
-30.0
-35.0
V (dB)
10^0
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
10^9
freq (Hz)

OTA Common Mode Feedback Gain and Phase vs Frequency



Standalone OTA Input-Referred Noise vs. Frequency

The dominant noise sources in the OTA are the two tail current sources and the two PMOS load devices. The gm's of these devices were 3.7e-3 and 4.6e-3, respectively. This leads to an output noise current of:

$$i_n^{\,2} = 4kT\gamma g_m = 5.10e-23 \text{ (NMOS)}$$

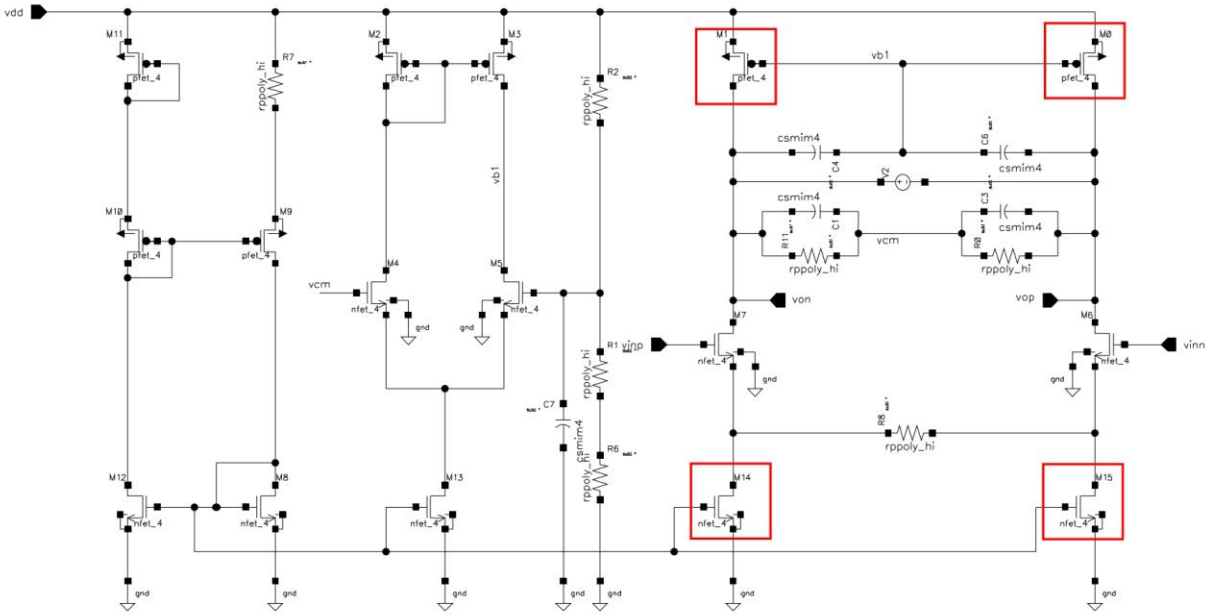
$$i_n^{\,2} = 4kT\gamma g_m = 4.11e-23 \text{ (PMOS)}$$

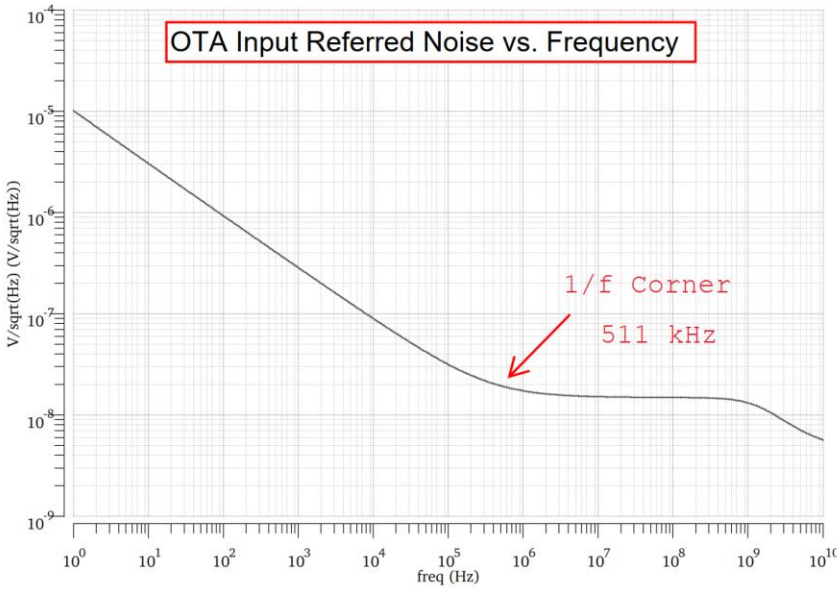
$$i_{n\_total}^{\,2} = 9.2e-23\frac{A^2}{Hz}$$

This output noise can be referred back to the input of the OTA by simply dividing it by the Gm of the OTA stage itself, which was designed to be around 5.0e-4 A/V. This leads to an input referred noise voltage of:

$$v_n = \frac{\sqrt{9.2e-23}}{5\times10^{-4}} = 19.1\frac{nV}{\sqrt{Hz}}$$

This agrees well with the simulated noise values above the 1/f corner where the thermal noise is dominant as seen in the simulated input referred results below.

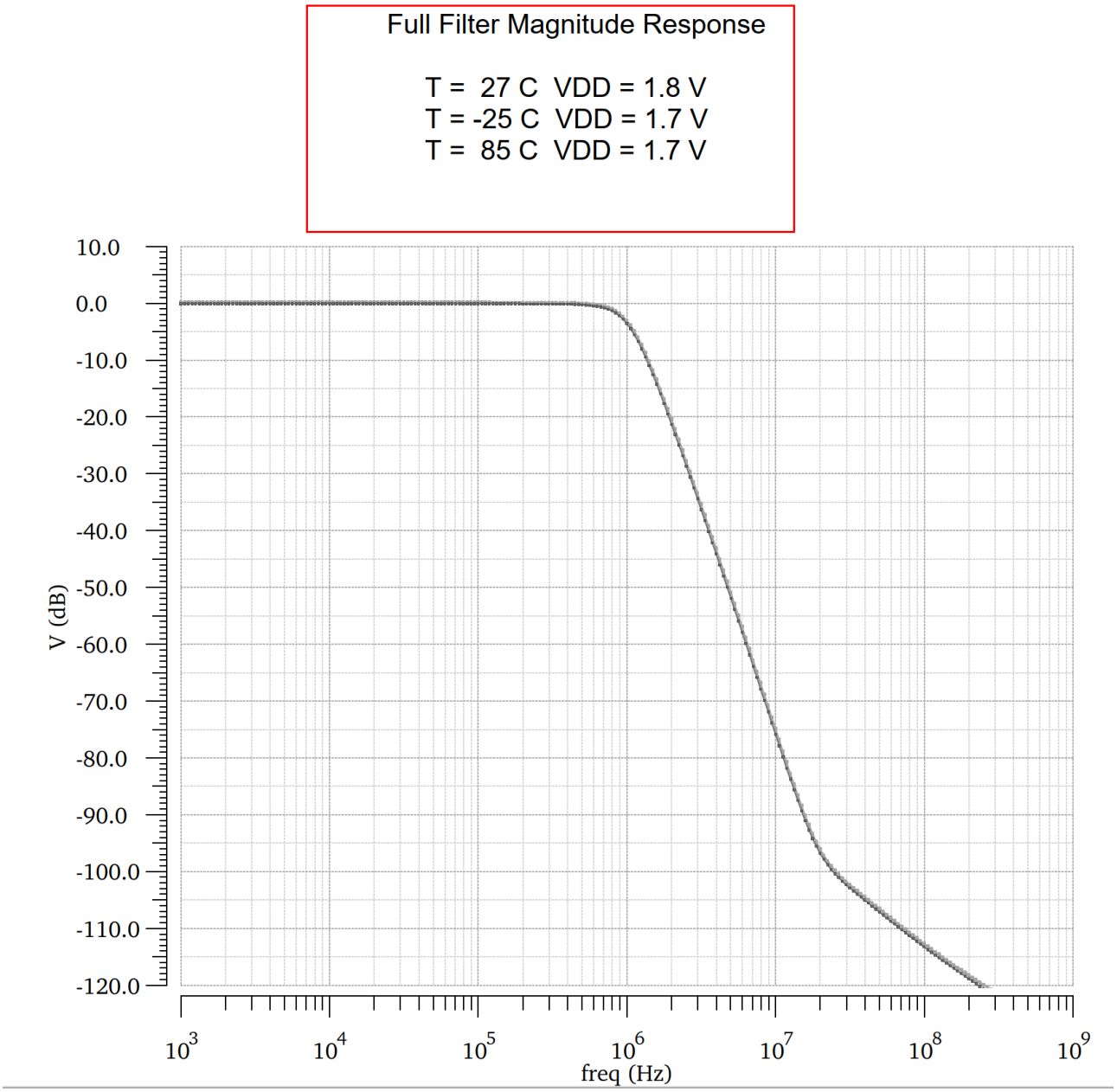


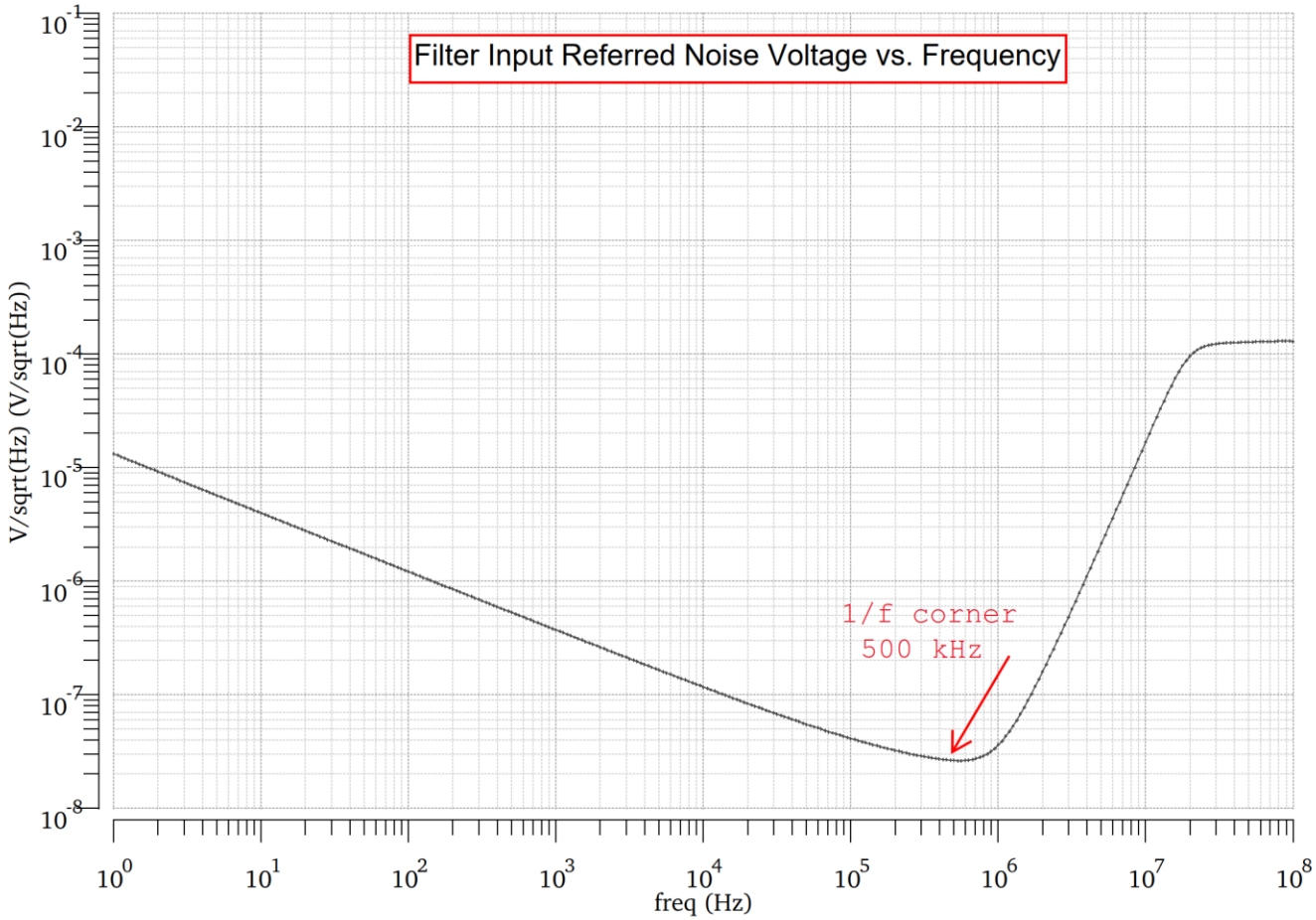


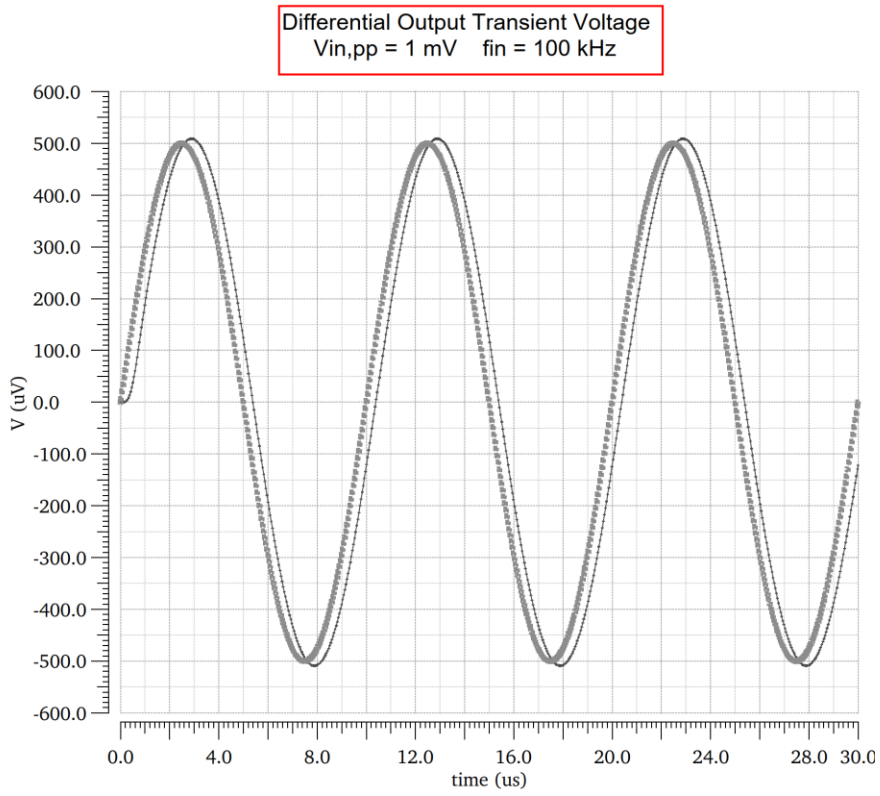
Noise Summary Dominant Contributors

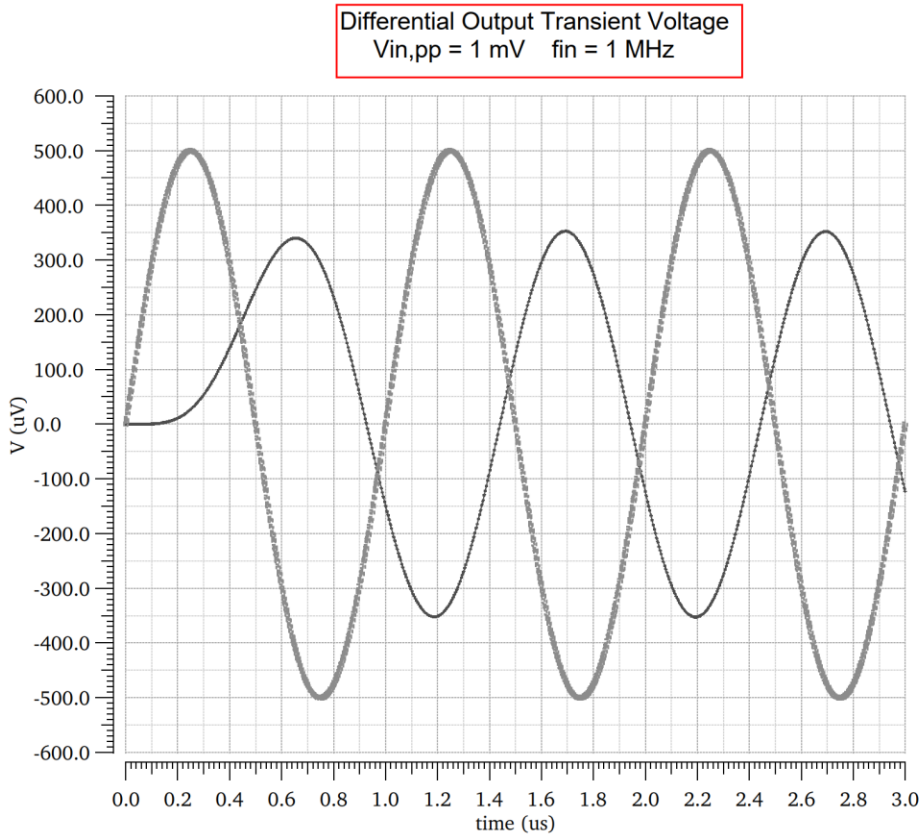
Device	Param	Noise Contribution	% Of Total
M0.mds	id	1.35102e-23	25.61
M1.mds	id	1.35102e-23	25.61
M15.mds	id	8.48769e-24	16.09
M14.mds	id	8.48769e-24	16.09
R8.r2	rn	3.9677e-24	7.52
R8.r1	rn	1.32257e-24	2.51
R8.r3	rn	1.32257e-24	2.51
M6.mds	id	8.26697e-25	1.57
M7.mds	id	8.26697e-25	1.57
M15.mds	fn	9.88611e-26	0.19
M14.mds	fn	9.88611e-26	0.19
M0.mds	fn	6.62859e-26	0.13
M1.mds	fn	6.62859e-26	0.13
M6.mds	fn	3.68725e-26	0.07
M7.mds	fn	3.68725e-26	0.07
R11.r2	rn	2.44534e-26	0.05
R0.r2	rn	2.44534e-26	0.05
R0.r3	rn	1.5629e-26	0.03
R11.r1	rn	1.5629e-26	0.03
R11.r3	rn	7.74342e-27	0.01

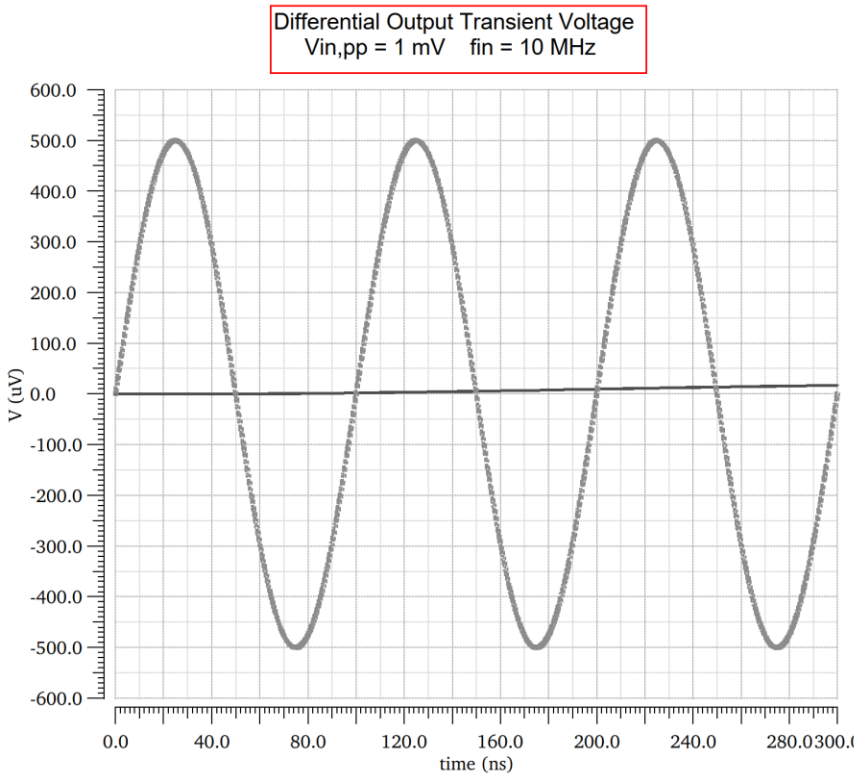
Spot Noise Summary (in A^2/Hz) at 50M Hz Sorted By Noise Contributors
Total Summarized Noise = 5.2762e-23
Total Input Referred Noise = 2.2525e-16
The above noise summary info is for noise data

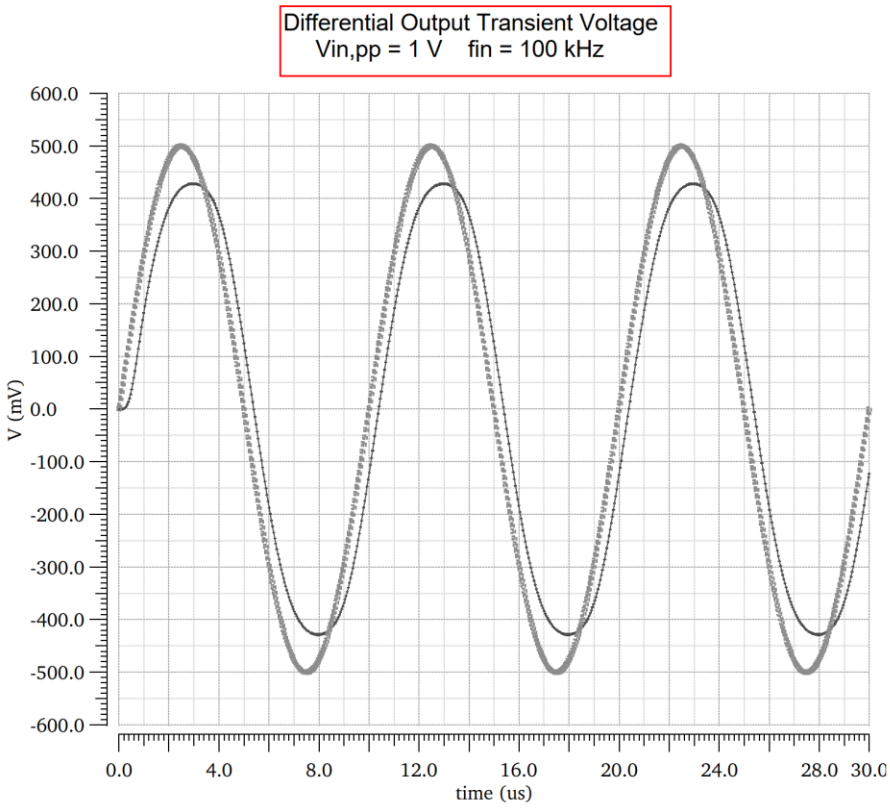

Full Filter Magnitude Response
T = 27 C VDD = 1.8 V
T = -25 C VDD = 1.7 V
T = 85 C VDD = 1.7 V
10.0
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
-60.0
-70.0
-80.0
-90.0
-100.0
-110.0
-120.0
V (dB)
10^3
10^4
10^5
10^6
10^7
10^8
10^9
freq (Hz)

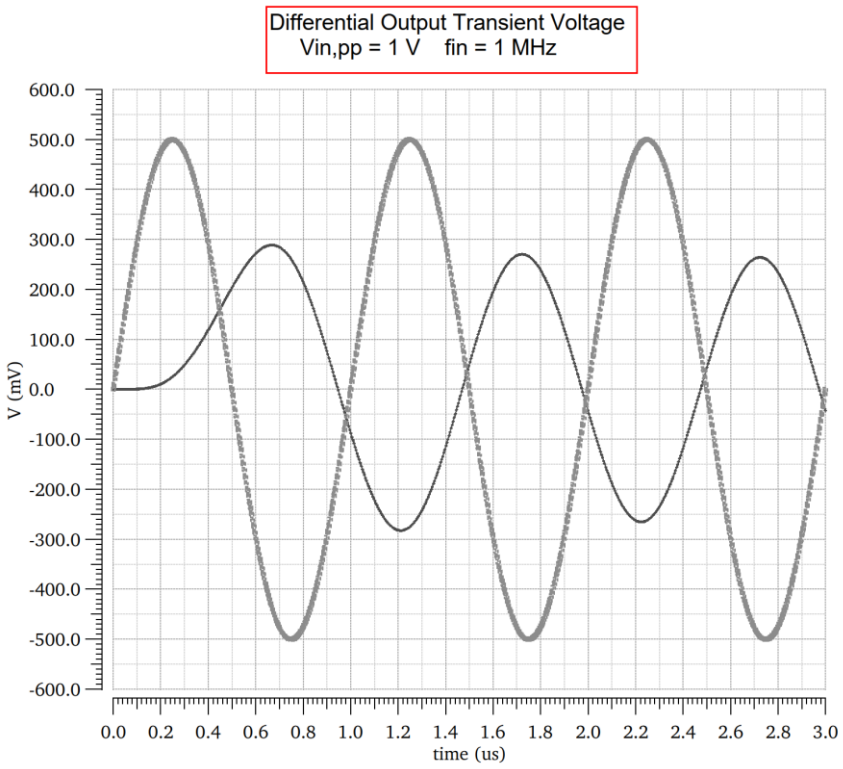

Filter Input Referred Noise Voltage vs. Frequency
V/sqrt(Hz) (V/sqrt(Hz))
freq (Hz)
1/f corner
500 kHz

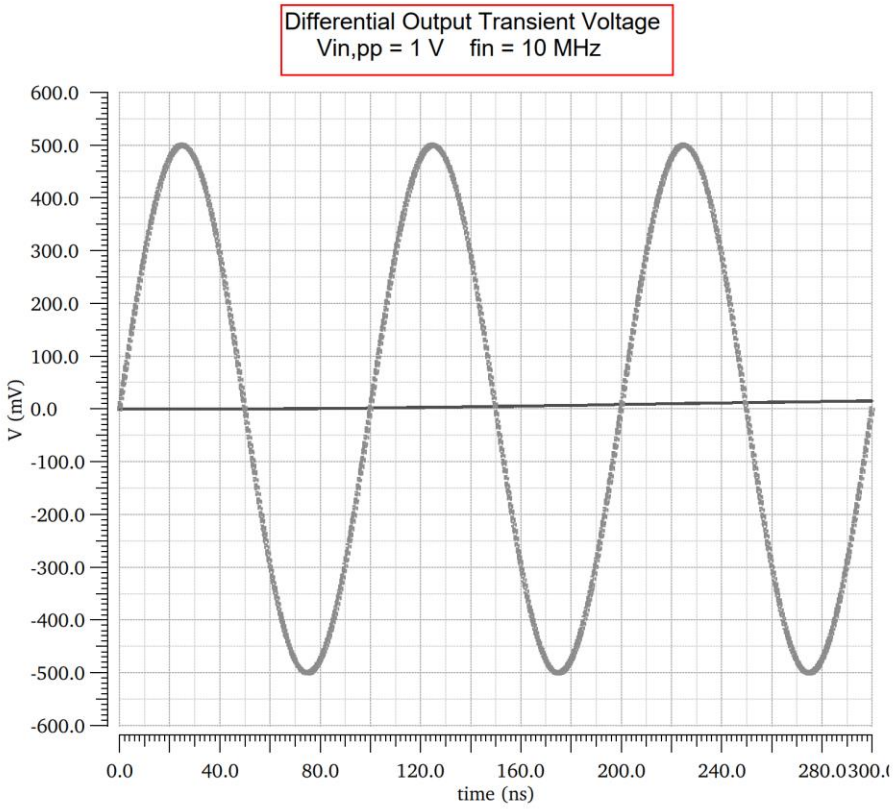

Differential Output Transient Voltage
Vin,pp = 1 mV fin = 100 kHz
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
-200.0
-300.0
-400.0
-500.0
-600.0
V (uV)
0.0
4.0
8.0
12.0
16.0
20.0
24.0
28.0
30.0
time (us)

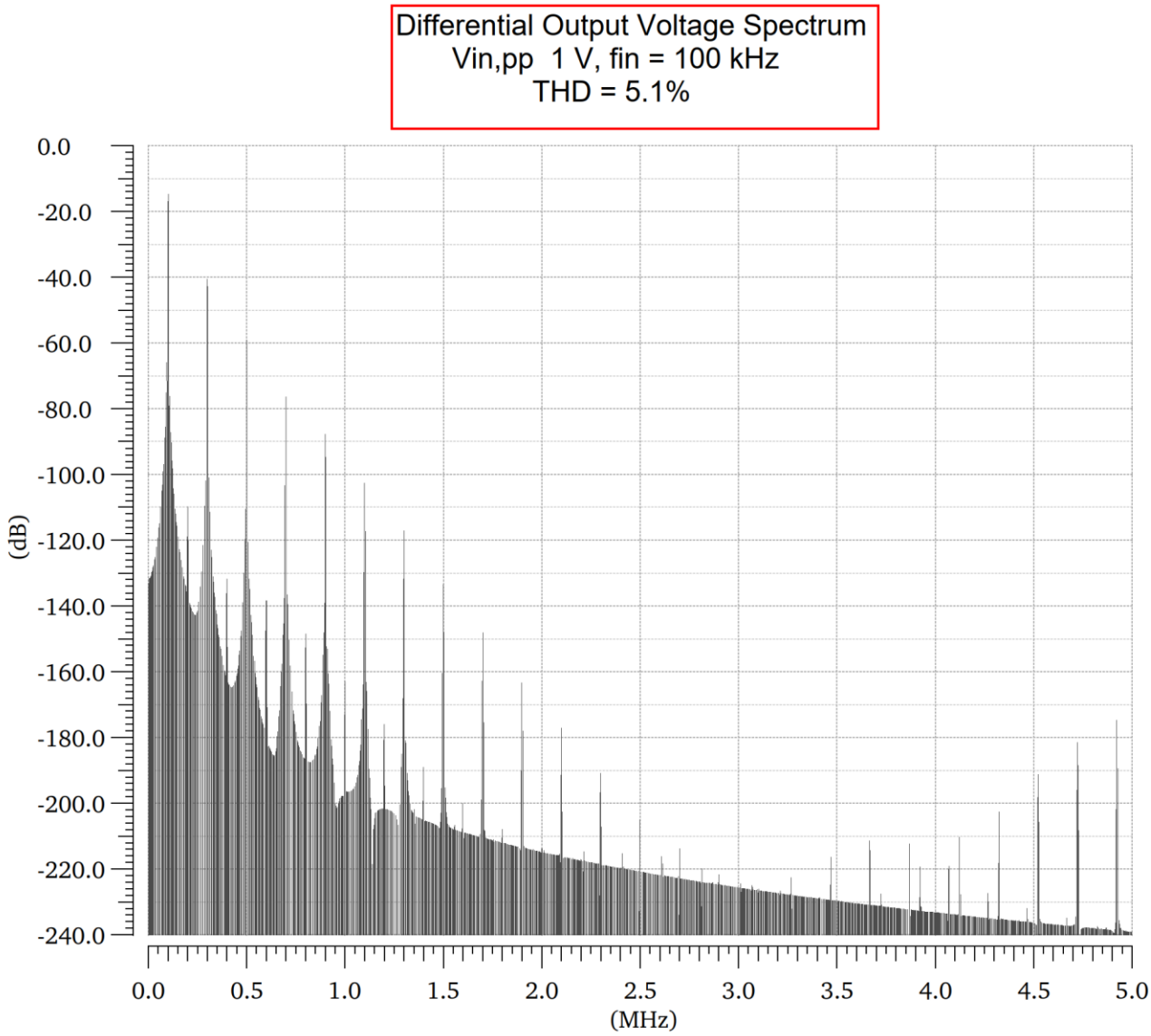

Differential Output Transient Voltage
Vin,pp = 1 mV fin = 1 MHz
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
-200.0
-300.0
-400.0
-500.0
-600.0
V (uV)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
time (us)


Differential Output Transient Voltage
Vin,pp = 1 mV fin = 10 MHz
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
-200.0
-300.0
-400.0
-500.0
-600.0
V (uV)
0.0
40.0
80.0
120.0
160.0
200.0
240.0
280.0
time (ns)

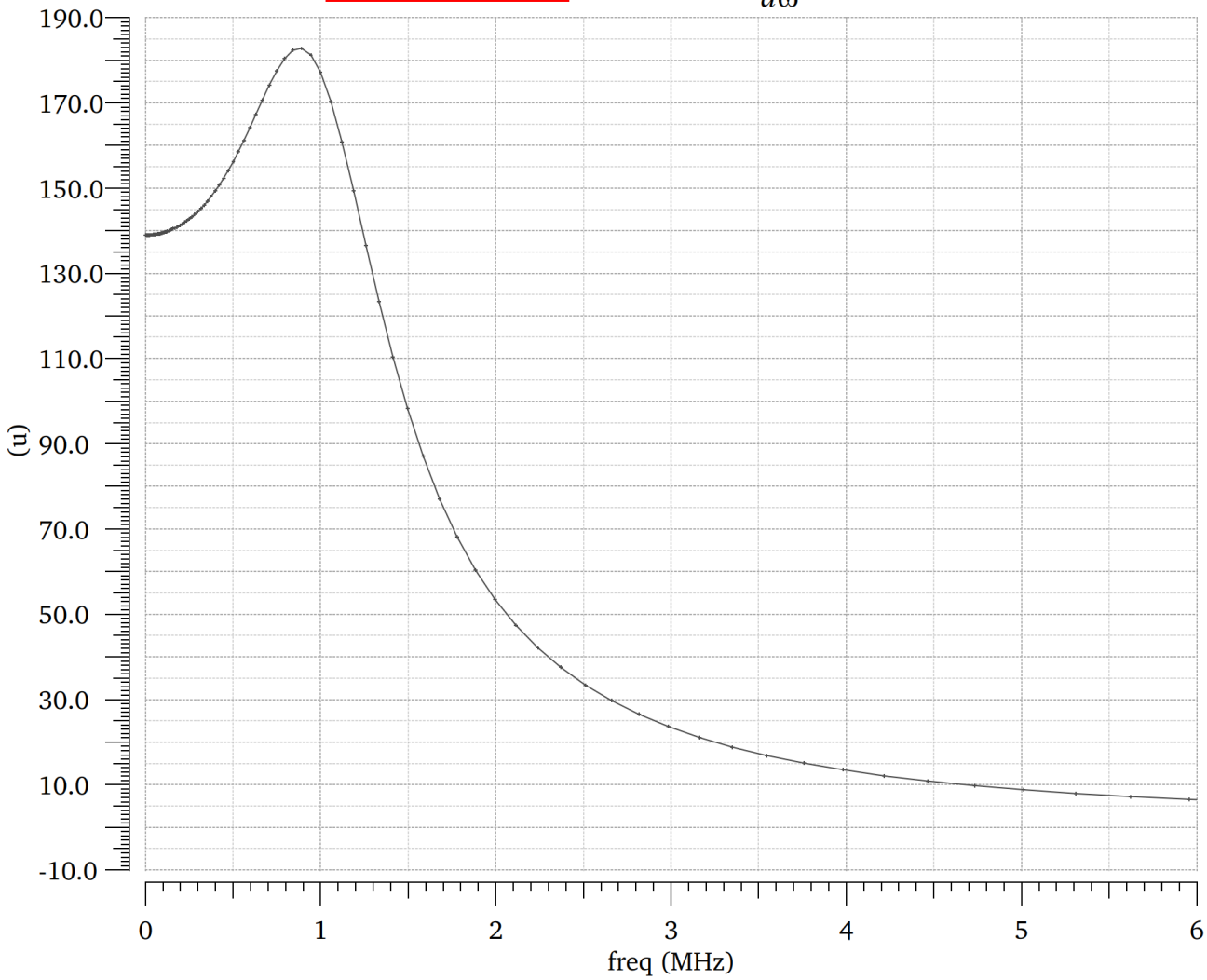

Differential Output Transient Voltage
Vin,pp = 1 V fin = 100 kHz
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
-200.0
-300.0
-400.0
-500.0
-600.0
V (mV)
0.0
4.0
8.0
12.0
16.0
20.0
24.0
28.0
30.0
time (us)


Differential Output Transient Voltage
Vin,pp = 1 V fin = 1 MHz
V (mV)
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
-200.0
-300.0
-400.0
-500.0
-600.0
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0
time (us)


Differential Output Transient Voltage
Vin,pp = 1 V fin = 10 MHz
V (mV)
600.0
500.0
400.0
300.0
200.0
100.0
0.0
-100.0
-200.0
-300.0
-400.0
-500.0
-600.0
0.0 40.0 80.0 120.0 160.0 200.0 240.0 280.0300.0
time (ns)


Differential Output Voltage Spectrum
Vin,pp 1 V, fin = 100 kHz
THD = 5.1%
0.0
-20.0
-40.0
-60.0
-80.0
-100.0
-120.0
-140.0
-160.0
-180.0
-200.0
-220.0
-240.0
(dB)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
(MHz)

Group Delay: $T_d(\omega) = -\frac{d\angle H(j\omega)}{d\omega}$



Conclusion

Overall, this was a challenging yet extremely inciteful design experience. Going from a passive filter structure and mapping it to an active integrated circuit implementation was a great learning experience and exposed me to many new design issues and circuit solutions. I found the issue of trying to operate with stringent headroom constraints especially challenging. It seems probable that many of the circuit structures I found in the literature were likely developed in higher voltage processes with multiple devices could be stacked with sufficient voltage range. Additionally, I found the dependency on temperature and supply voltage to be quite miniscule, with only small differences across the process corners that were tested. I also found that designing using a systematic methodology—while definitely more work in the beginning stages of the design—proved to be extremely useful. In circuit design it can be very tempting to try to assemble a complicated structure all at once, but taking the time to coherently design a circuit in small, incremental steps is truly the superior way. I probably learned as much from the things that didn't work as I did from the structures that I eventually settled on in the final design.

References

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