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Final Project: Operational Amplifier

Design Rationale

I tried several topologies throughout the design of my operational amplifier. I tried implementing a telescopic structure as well as a folded cascode version. While these topologies provided great bandwidth and phase margin, I struggled to reach the target DC gain of 60 dB. It seemed to be difficult to bias these circuits as there was not much headroom to work with. After many attempts and different implementations, I arrived at a basic topology which is a two-stage design, consisting of a differential pair followed by another single ended gain stage. The benefits of the topology that I chose are that there is an overall gain multiplication of the two stages, so each stage is only required to have a gain of 31. Additionally, the output stage does not need any cascodes, which thus allows for a larger output range. Similarly, the input stage does not need any cascodes, which yields a better common-mode input range. For bias generation of current, I chose to implement the supply independent current source that we learned in lecture, with a diode connected NMOS instead of a BJT. I also implemented a compensation resistor in series with the normal compensation capacitor between the first and second stages, which provided better phase margin by moving the zero to partially compensate for the second pole, and this also improved bandwidth. This basic amplifier topology is inspired from my original project 1 design, which came from “MOS Operational Amplifier Design—A Tutorial Overview” which is referenced below [1]. This paper was also useful for bandwidth compensation.

Hand Analysis

DC Gain:

The total gain of the amplifier is the gain of the two individual stages multiplied together.

$$A_1 \approx g_{m1}(r_{o2} \parallel r_{04})$$
$$A_2 \approx g_{m6}(r_{o6} \parallel r_{07})$$
$$A_{Total} = A_1 * A_2 = g_{m1}g_{m6}(r_{o2} \parallel r_{04}) * (r_{o6} \parallel r_{07})$$
$$\boxed{A_{Total} = 477.0 = 53.6dB}$$

Opamp Unity Gain-Bandwidth Product:

There are two main poles in this circuit.

$$p_1 = \frac{1}{2\pi C_c(1+A_2)(r_{o2} \parallel r_{04})}$$
$$p_2 = \frac{g_{m6}C_c}{2\pi(C_1C_2 + C_1C_c + C_2C_c)}$$

$$A_{DC} = A_1A_2 = g_{m1}g_{m6}(r_{o2} \parallel r_{04}) * (r_{o6} \parallel r_{07})$$

$$UGBW = A_1A_2p_1 = \frac{g_{m1}g_{m6}(r_{o2} \parallel r_{04}) * (r_{o6} \parallel r_{07})}{2\pi(r_{o2} \parallel r_{04}) * C_1(1+A_2)}$$

$$\boxed{UGBW = 3.1GHz}$$

Phase Margin:

$$\phi_m = 90 - \tan^{-1}\left(\frac{A_{DC}f_{p1}}{f_{p2}}\right) = 90 - \tan^{-1}\left(\frac{g_{m1}g_{m6}(r_{o2} \parallel r_{04}) * (r_{o6} \parallel r_{07}) \dfrac{1}{2\pi C_c(1+A_2)(r_{o2} \parallel r_{04})}}{\dfrac{g_{m6}C_c}{2\pi(C_1C_2 + C_1C_c + C_2C_c)}}\right)$$

$$\boxed{\phi_m = 75.6°}$$

Slew Rate:

$$\text{SR+} = \frac{dV}{dt} = \frac{I_{M6}}{C_c + C_L + C_2} = \frac{56.3mA}{7.2p + 1p + 2p} \rightarrow \boxed{\text{SR+} = 5.5 \times 10^9}$$

$$\text{SR-} = \frac{dV}{dt} = \frac{gm_6 * (0.5)}{C_c + C_L + C_2} = \frac{0.189}{7.2p + 1p + 2p} \rightarrow \boxed{\text{SR-} = 18.5 \times 10^9}$$

Input Common Mode Range:

$$V_{da} = V_{in} + V_{gs\_m1}$$
$$(V_{dd} - V_{da}) > V_{dsat\_m5}$$
$$V_{dd} - (V_{in} + V_{gs\_m1}) > V_{dsat\_m5}$$
$$V_{dd} - V_{in} - V_{TN} - V_{dsat\_m1} > V_{dsat\_m5}$$
$$V_{in} < V_{dd} - V_{TN} - V_{dsat\_m1} - V_{dsat\_m5}$$
$$V_{in} < V_{dd} - V_{TN} - 2V_{dsat}$$
$$V_{in} < 1.6 - 0.368 - 2(0.316)$$
$$\boxed{V_{in} < 0.6V}$$

$$V_{gs\_m1} < V_{in} + V_{TP}$$
$$V_{TN} + V_{dsat\_m3} < V_{in} + V_{TP}$$
$$V_{in} > V_{TN} - V_{TP} + V_{dsat\_m3}$$
$$\boxed{V_{in} > 0.28}$$

$$\boxed{ICMR = 0.6 - 0.28 = 0.32}$$

Common Mode Rejection Ratio:

$$\Delta Vout = \left[\frac{\Delta V_{cm}}{r_{o5}} \cdot \frac{1}{g_{m3}} \right] A_2$$

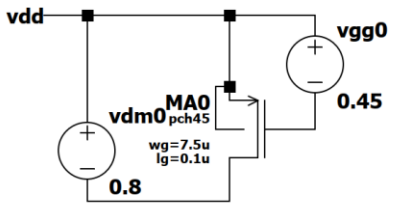
$$\Delta Vout = \Delta V_{cmi} \left(\frac{1}{g_{m3} r_{o5}} \right) g_{m6} \left(r_{o6} \| r_{o7} \right)$$

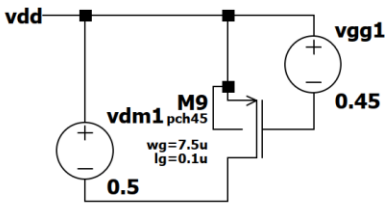
$$CMRR = \frac{\frac{g_{m6} \left(r_{o6} \| r_{o7} \right)}{g_{m3} r_{o5}}}{g_{m1} g_{m6} (r_{o2} \| r_{04}) \left(r_{o6} \| r_{o7} \right)} = \frac{1}{g_{m1} g_{m3} r_{o5} (r_{o2} \| r_{04})}$$

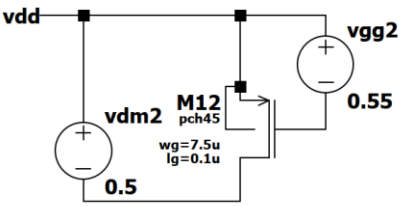
$$\boxed{CMRR = 0.0046 = 47dB}$$

Circuit and Circuit Test Benches

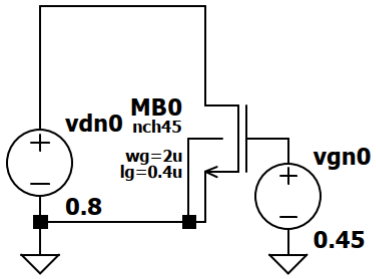
The following circuits were used to determine the intrinsic parameters of the nmos and pmos transistors. The parameters shown below the three circuits are extracted from the measured currents in the test structures.

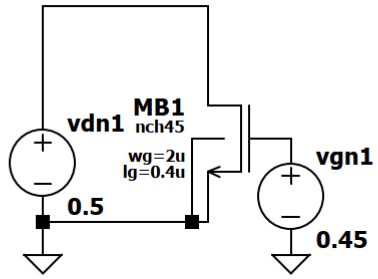


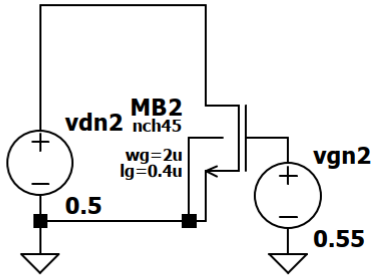




LamdaP	230.48406m
VTP	353.1209m
KPP	32.936106µA

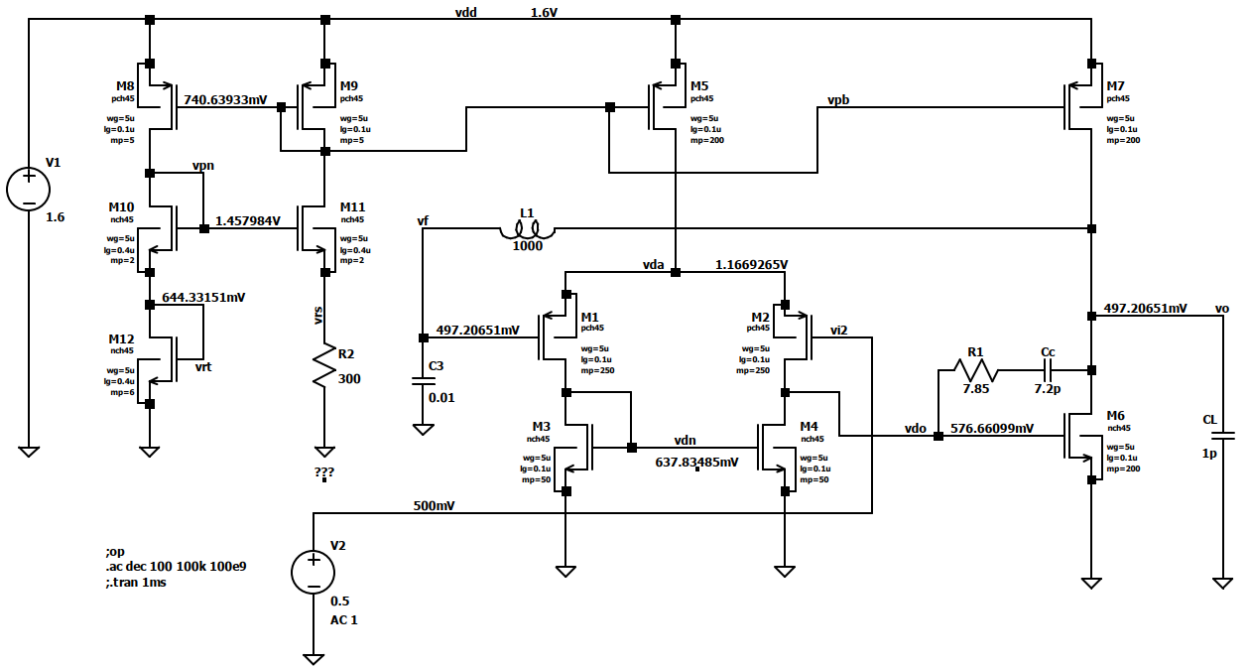




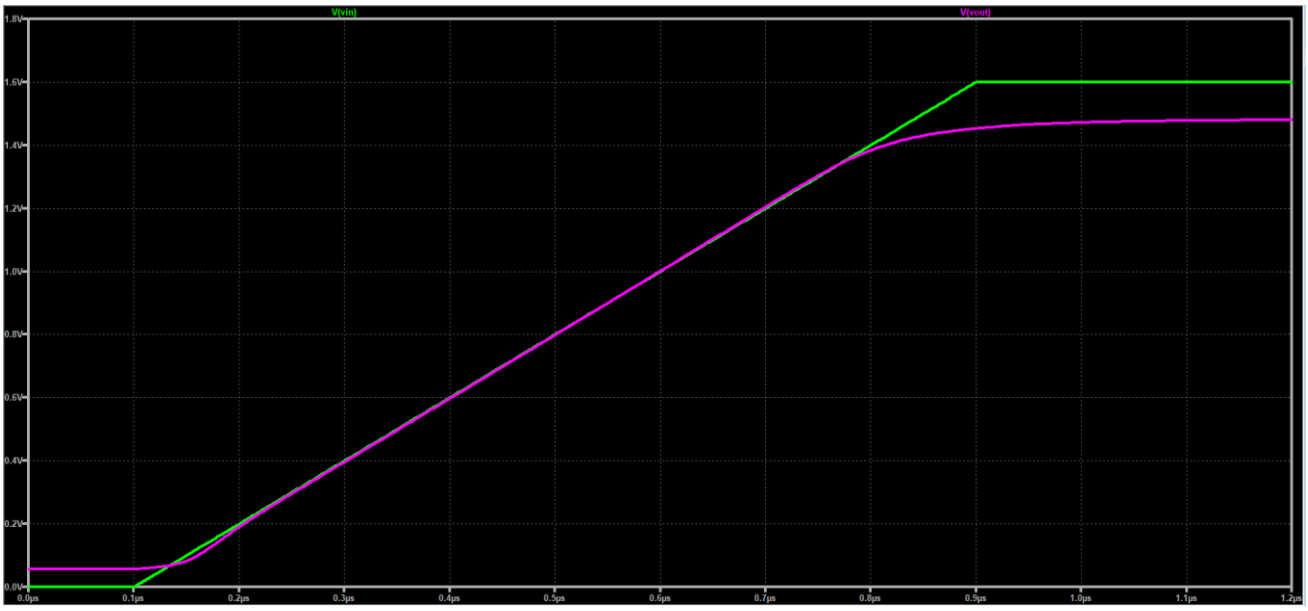


LamdaN	50.985821m
VTN	368.49251m
KPN	127.03458µA

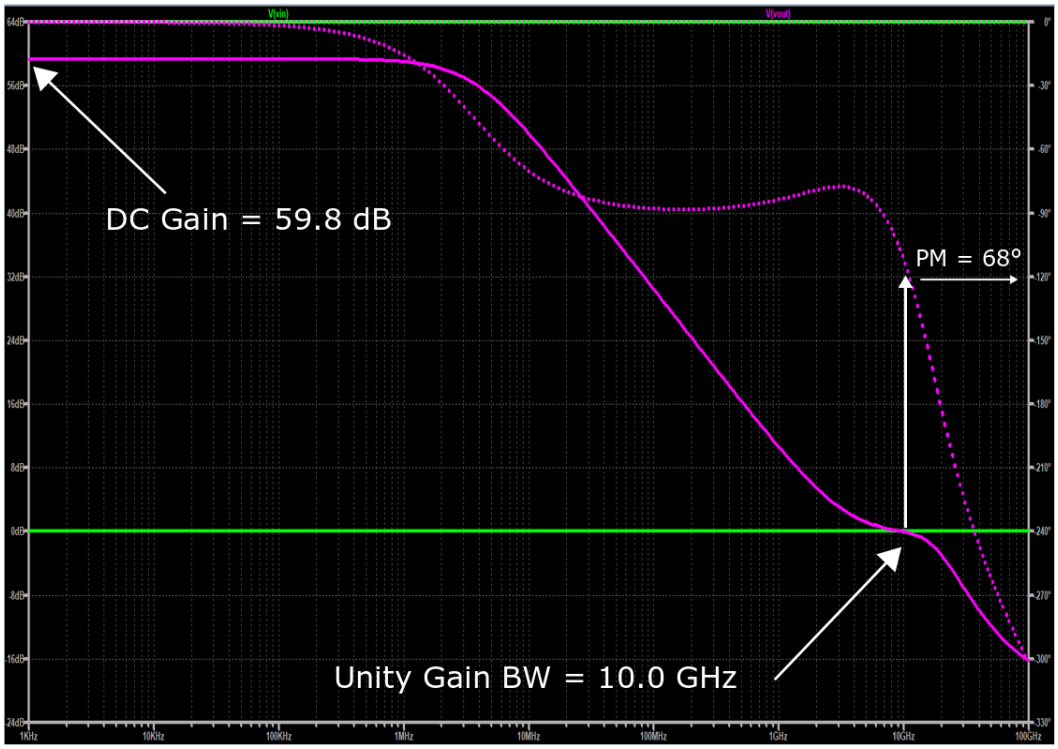
Main Opamp with DC Operating Point



Simulation Result DC Sweep

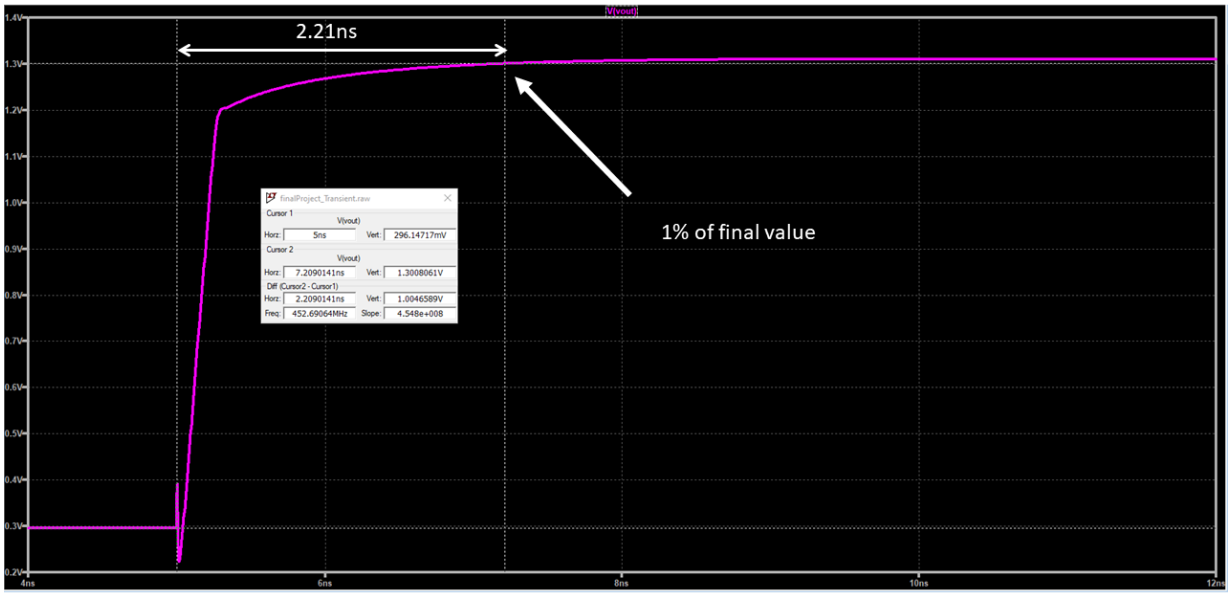


Simulation Result AC Response

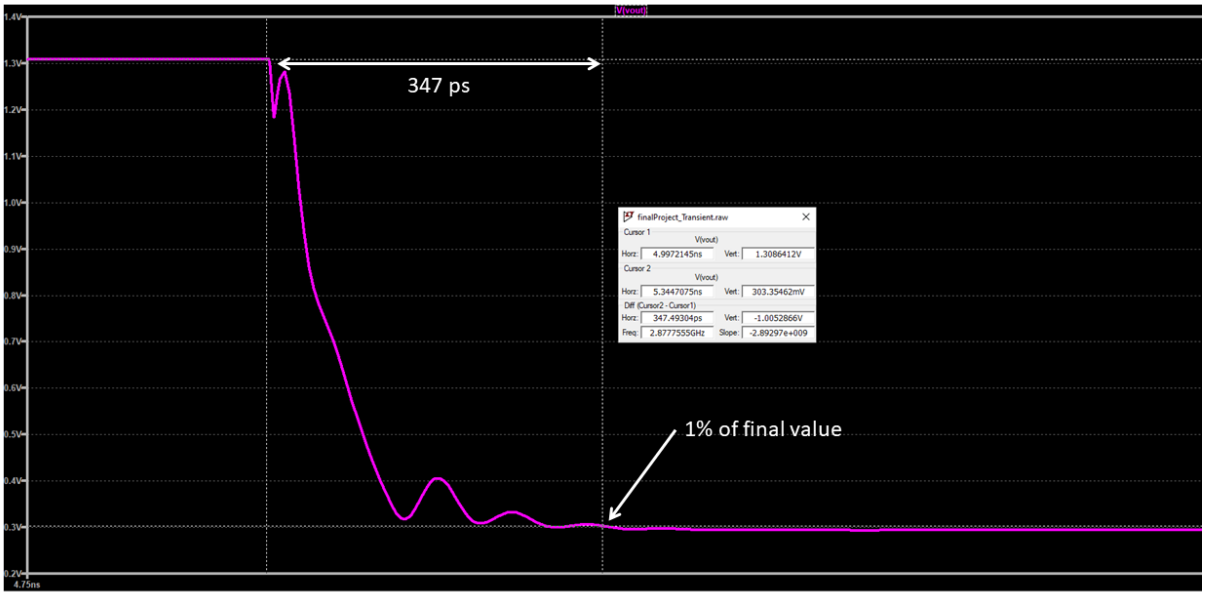


Transient Response

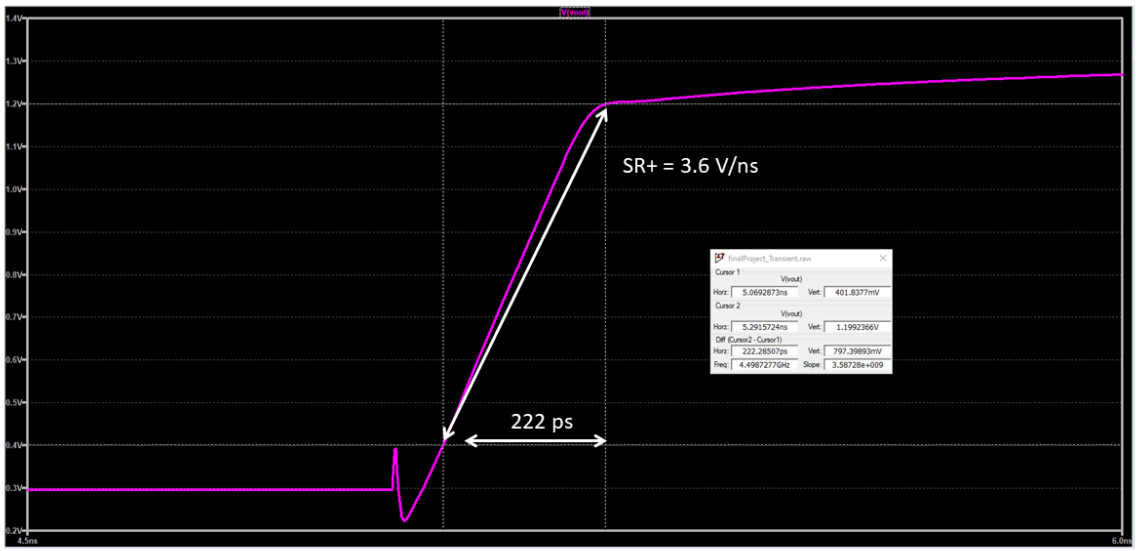
Settling Time (+) :



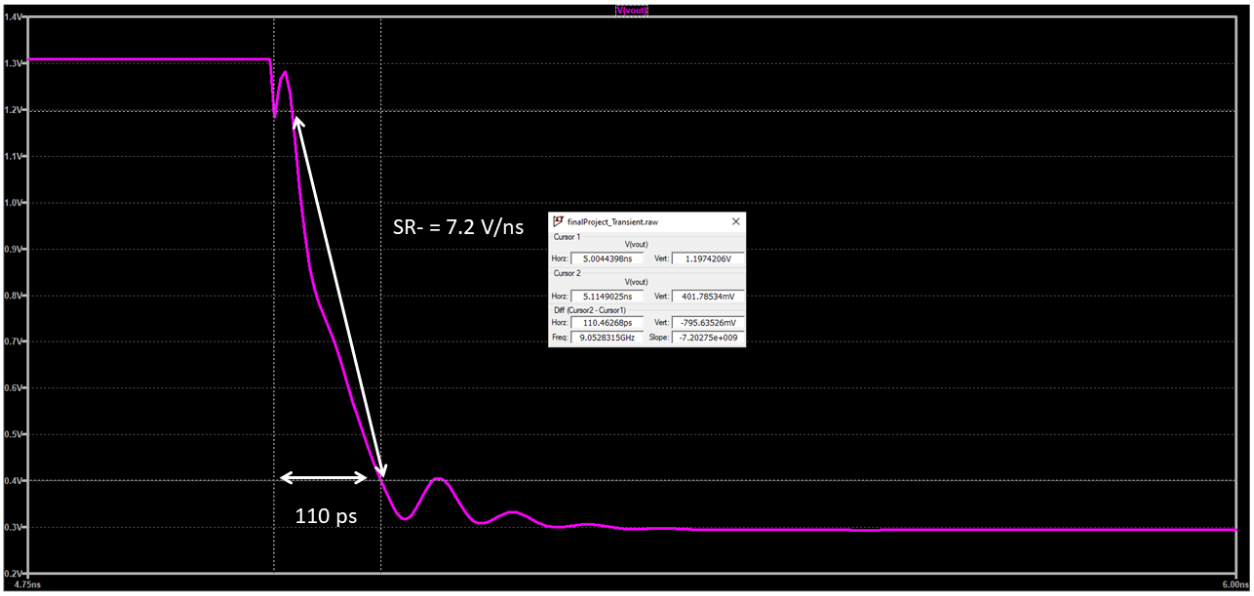
Settling Time (-) :



Slew Rate (+) :



Slew Rate (–) :


V(vout)
1.4V
1.3V
1.2V
1.1V
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
4.75ns
6.00ns
SR- = 7.2 V/ns
110 ps
finalProject_Transient.raw
Cursor 1
V(vout)
Horz: 5.0044398ns
Vert: 1.1974206V
Cursor 2
V(vout)
Horz: 5.1149025ns
Vert: 401.78534mV
Diff (Cursor2 - Cursor1)
Horz: 110.46268ps
Vert: -795.63526mV
Freq: 9.0528315GHz
Slope: -7.20275e+009

Summary Tables

Device Sizes				
Transistor	Width	Length	Resistor	Size (ohm)
M1	1250u	0.1u	R1	7.85
M2	1250u	0.1u	R2	300
M3	250u	0.1u		
M4	250u	0.1u	Capacitor	Size
M5	1000u	0.1u	Cc	7.2p
M6	1000u	0.1u	CL	1p
M7	1000u	0.1u		
M8	25u	0.1u	Parasitic Capacitances	
M10	10u	0.4u	C1	2.2p
M11	10u	0.4u	C2	2p
M12	30u	0.4u		

	Vgs	Vds	Vgs-Vt	Id	gm	r0
M8	859.36067mV	142.01603mV	506.23977mV	711.41985µA	3.37383µmohm-1	6.111477Kohm
M9	859.36067mV	859.36067mV	506.23977mV	1.3705342mA	4.6827926mohm-1	3.1723598Kohm
M5	859.36067mV	433.0735mV	506.23977mV	51.092796mA	180.82973mohm-1	85.096687ohm
M7	859.36067mV	1.1027935V	506.23977mV	56.276917mA	189.78205mohm-1	77.257741ohm
M10	813.65246mV	813.65246mV	445.15995mV	708.77129µA	670.87239µohm-1	27.664556Kohm
M11	1.0461585V	328.81388mV	677.66601mV	1.3705698mA	932.90505µohm-1	14.306344Kohm
M12	644.33151mV	644.33151mV	275.839mV	708.90039µA	670.93349µohm-1	27.659518Kohm
M1	669.71999mV	529.09166mV	316.59909mV	25.657116mA	143.26793mohm-1	169.45888ohm
M2	666.9265mV	590.26551mV	313.8056mV	25.435684mA	142.64836mohm-1	170.93411ohm
M3	637.83485mV	637.83485mV	269.34234mV	25.655923mA	127.6382mohm-1	764.26184ohm
M4	637.83485mV	576.66099mV	269.34234mV	25.434487mA	127.08619mohm-1	770.91563ohm
M6	576.66099mV	497.20651mV	208.16848mV	56.277007mA	378.07882mohm-1	348.4166ohm

	Comparison of Results		
			% Difference
DC Gain	Hand Analysis	53.6 dB	0.100 = 10.0%
	Simulation	59.8 dB	
UGBW	Hand Analysis	3.1 GHz	0.069 = 69%
	Simulation	10.0 GHz	
Phase Margin	Hand Analysis	75.6 deg	0.154 = 5.4%
	Simulation	65.5 deg	
SR+	Hand Analysis	5.50E-09	0.527 = 52.7%
	Simulation	3.60E-09	
SR-	Hand Analysis	1.85E+10	0.61 = 61%
	Simulation	7.20E+09	
ICMR	Hand Analysis	0.32V	0.030 = 3.0%
	Simulation	0.33V	
CMRR	Hand Analysis	47 dB	0.022 = 2.2%
	Simulation	46 dB	

Specification/Performance Table

Parameter Description	**Desired**	**Achieved**	**Unit**
Power Supply(C_L)	0.8-1.6	1.6	V
Ground Supply(V_{ss})	0	0	V
Output Load (C_L)	1	1	pF
Opamp DC Gain (A_{v0})	60	59.8	dB
Opamp Unity Gain-Bandwidth Product (UGBW)	10	10	GHz
Phase Margin (φ)	> 65	68	Degree
Positive Settling Time (0.01% of 1V input step)	< 5	2.21	ns
Negative Settling Time (0.01% of 1V input step)	< 5	0.347	ns
Supply Current Consumption (I_{DD})	-	109.5	mA
Power Consumption (V_{DD}*I_{DD})	-	175.1	mW
Positive Slew Rate (SR+)	> 1	3.6	V/ns
Negative Slew Rate (SR-)	> 1	7.2	V/ns
Input Common-Mode Range (ICMR)	> 0.8	0.33	V
Input Common-Mode Range (ICMR) (A_{v0} > 50 dB)	> 0.8	0.98	V
Common Mode Rejection Ratio @ DC (CMRR)	> 60	46	dB

Discussion of Results

Overall, the hand analysis and simulation results for the gain compared well with each other with the exception of the bandwidth and slew rate. All of the other calculations were within 10% of the simulation values, which is reasonable given that many of the equations are based on the simplified square law model. Additionally, the intrinsic parameters of the MOS devices used in the hand analysis do not account for many of the nonidealities that the device models do. The bandwidth was likely off due to a high sensitivity to the compensation resistor placed in series with the compensation capacitor. In the end, I had to rely on the simulator for the optimum sizing of the resistor for maximum phase margin. For the slew rate, the large variance was likely due to poor behavior near the extremes of the operating range. This complicated behavior was difficult to calculate and the simplified equations I was using in the analysis did not model those effects. Overall, the design seemed to be successful as it met almost every specification except for the ICMR, which was a result of V_{dsat} being high on many of the devices which led to headroom issues. I believe the design could easily meet this spec if the gain, bandwidth, or phase margin requirements were lowered, but I found it difficult to meet the ICMR > 0.8V desired spec while simultaneously still meeting these three other parameters.

References

[1] P. Gray and R. Meyer, "MOS operational amplifier design-a tutorial overview", *IEEE Journal of Solid-State Circuits*, vol. 17, no. 6, pp. 969-982, 1982. Available: 10.1109/jssc.1982.1051851.

[2]P. Gray and R. Meyer, *Analysis and design of analog integrated circuits*, 5th ed. New York: Wiley, 2010.