Voltage Controlled Oscillator in 0.18u CMOS

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Abstract**—A relaxation voltage controlled oscillator is proposed as a building block for application in a phased-locked loop. The sub-circuit blocks are systematically designed and laid out for straightforward integration into a larger system.**

I. INTRODUCTION

Voltage controlled oscillators are widely used in mixed signal integrated circuits and are one of the central building blocks of phased locked loops which are used in most on-chip clock generators. In the design of a voltage-controlled oscillator (VCO), there are two main types: harmonic oscillators and relaxation oscillators. Depending on the application, each type of VCO exhibits particularly advantageous properties. Harmonic oscillators are based on the physical properties, namely the resonance of certain energy components such as inductors and capacitors. Despite the high purity signals they are capable of producing, the designs are typically bulky, and the tuning range is narrow. Relaxation oscillators are based on a chain of delay elements—like a ring oscillator—and offer many desirable characteristics such as simple and smaller designs, as well as wider tuning ranges. For this particular design, a relaxation oscillator is built using a series of five delay cells, which will be discussed. The design goal of this project was to implement a VCO with an operating voltage range of down to half supply (0.9V) and oscillation frequency range of around 1 GHz. In the layout phase of the project, several techniques were utilized which will be discussed in a later section. For an ideal VCO, the relationship between the input control voltage and the output frequency should be linear.

II. ARCHITECTURE

Figure 1 below shows the chosen topology that is being proposed for this design. This structure uses a single control voltage, Vctrl, which is the supply for the five delay cells as well as the inverters immediately following the delay cells. An odd number of delay cells was purposely chosen to eliminate the possibility of the oscillator getting in a locked state. The inverters immediately following the five delay cells as well as the two inverters at each of the outputs serve the purpose of buffering. The outputs are also AC-coupled with the use of two capacitors, two resistors, and one inverter for each of the outputs. The first capacitor is essentially a DC-blocker, and the inverter and other passive devices set the common mode to mid-supply. This is accomplished through using VDD (1.8V) to control these inverters, rather than Vctrl. The architecture of every delay cell is identical and consists of four cross-coupled inverters. The schematic as well as the layout of the delay cell will be shown in a later section.

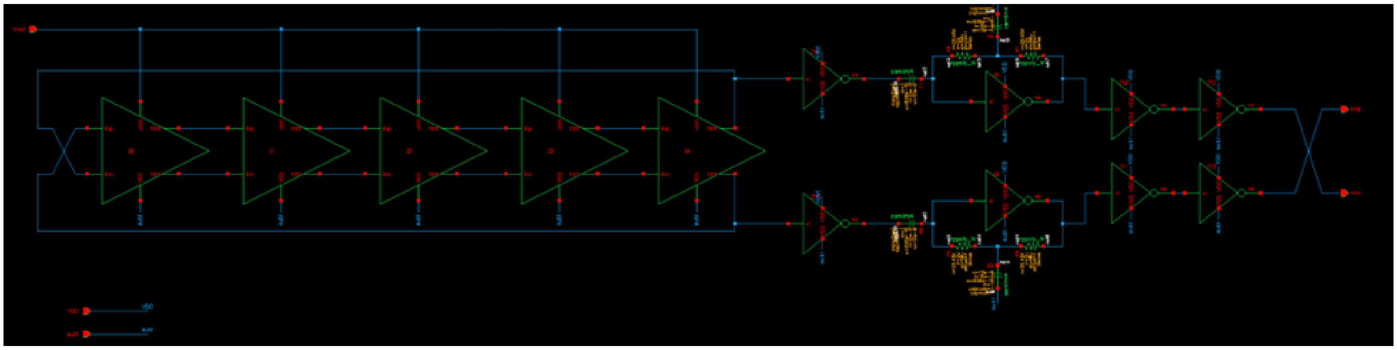


Figure 1:Full VCO with Buffering and AC-Coupling

III. DESIGN STRATEGY AND SPECIFICATIONS

There are several important metrics considered in the design of a VCO. To describe the performance, factors such as power consumption, signal purity, tuning range, and noise rejection are all important. Additionally, the VCO gain is an important aspect of VCO design, which is a measure of the ratio of the range of the output frequency to the range of the input control voltage. For the layout portion of the design, the main objective was to achieve a relatively square design with as much symmetry as possible. As aforementioned, one potential complication that can arise in oscillator design is getting in a locked state. Having some asymmetry in the layout, at least in this regard, is actually beneficial as start up problems will be less likely to occur. Moreover, the output signal purity of a VCO is of utmost importance and depends on several factors, many of which have been discussed. The ability of power supply rejection is also critical for good signal performance, and as such large power supply rails were used and ample well taps. One additional step that was taken during the layout design was placing components methodically in such a way that nodes with higher sensitivities to parasitics had the shortest traces. Some trace widths were also made wider to avoid dogbone errors.

One technique that made the whole layout process and routing much easier was building each smaller cell with identical heights: both in terms of the overall height of cell from the power and ground rails as well as the heights of inputs and outputs. This made routing much easier, symmetry more achievable, and the overall design experience smoother. For the routing, I chose to use metal layers 1-4, and each metal layer was used perpendicular to the preceding and succeeding one. This technique proved to be very helpful in keeping track of traces and connections and used die space effectively and efficiently. For this design, poly resistors and MIM capacitors were used.

IV. TRADEOFFS

As with any circuit design, several tradeoffs arose throughout the course of this project. The signal purity of a VCO is largely dependent on the phase noise and jitter, which are both proportional to the dissipated power. Scaling device sizes up for better performance and matching also introduced the tradeoff of area consumption. Transistor gate lengths are also an important factor in relation to speed, and minimum gate lengths were used throughout the course of this design.

V. SCHEMATIC DESIGN

Figure 2 shows the schematic for the single inverter that was used in this VCO. Based on the rise and fall times that were measured earlier in the semester, the PMOS device was sized three times that of the NMOS device.

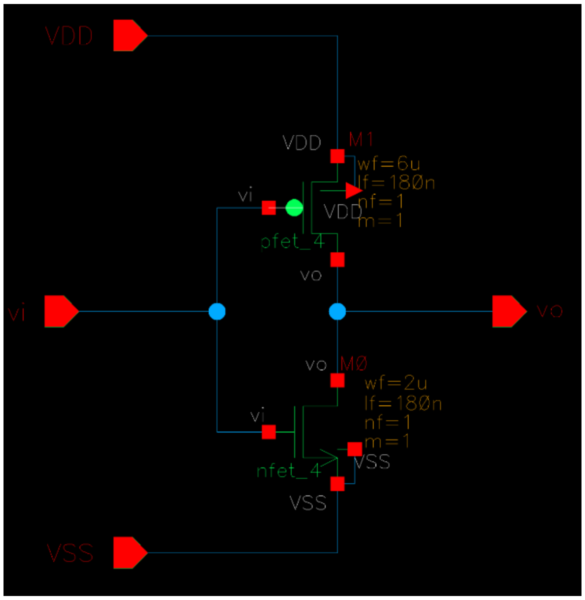


Figure 2: Single Inverter

For the delay cell, the same ratio was used, but sizes were scaled up. Figure 3 shows the schematic of a delay cell.

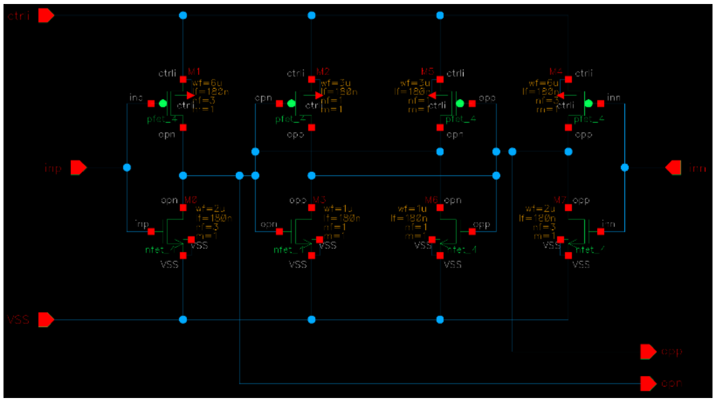


Figure 3: Delay Cell

The delay cell consists of four inverters that are cross coupled which form a loop. By routing the positive output to the negative input terminal in the chain of these delay cells, the oscillation is achieved. It should be noted that the two outer inverters in the delay cell are sized significantly larger than the inner ones, and that the same number of fingers in each of the individual inverters is used. One benefit of this delay cell design, which uses the control voltage as the PMOS bulk, is that there is no Vth variation and thus the output frequency changes linearly.

VI. LAYOUT DESIGN

Figures 4 and 5 show the layout of the single inverter and the delay cell, respectively. It should be noted that the size of each of these cells is identical to each other. With the same height, the power and ground rails had straightforward connections which also helped in keeping the overall design symmetric. It should also be noted the directions in which each metal layer runs. Aside from the power and ground rails, meal one is strictly used for vertical routing, while metal two is used for horizontal routing and so on. This methodology helped make the layout process much smoother, and it was relatively simple to route the necessary connections. Figures 6-10 show the full layout design starting from the lower layers and successively adding an additional metal layer with each figure, which makes visualizing each of the metal layers much easier to follow.

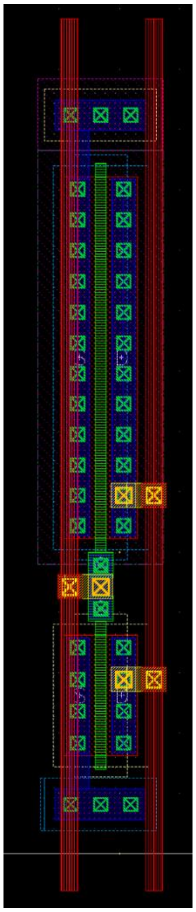


Figure 4: Single Inverter

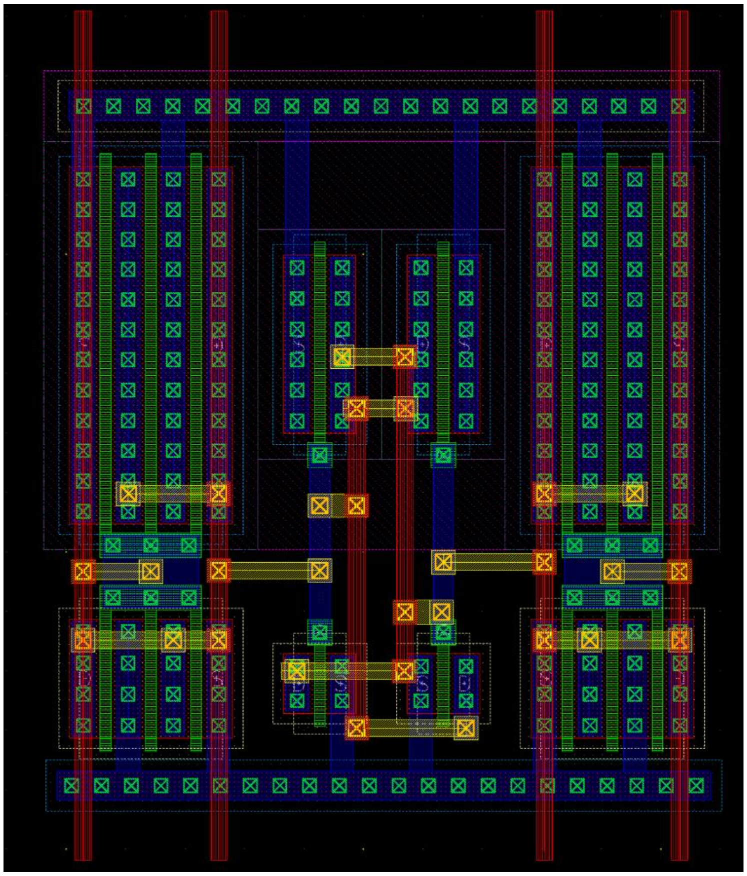


Figure 5: Delay Cell

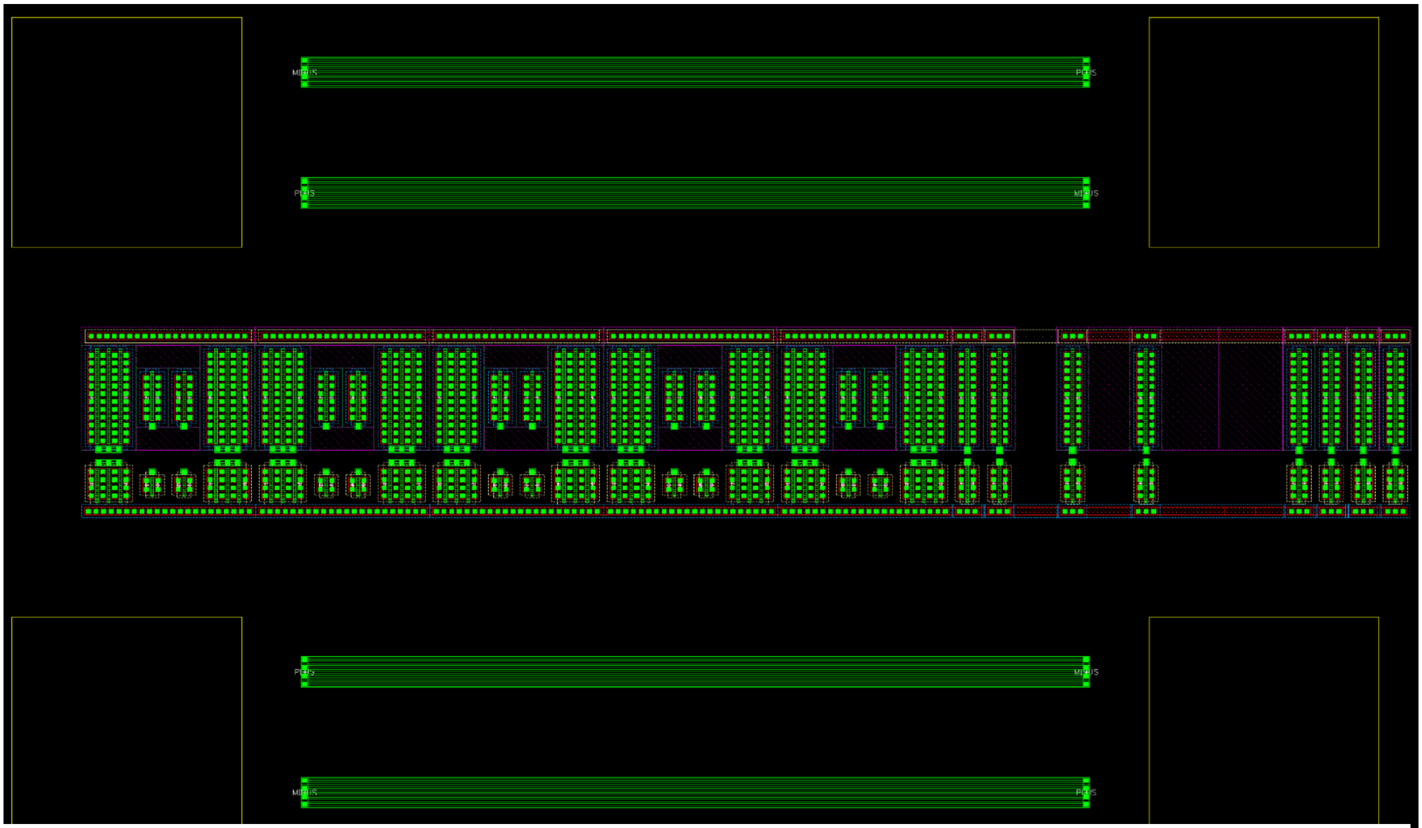


Figure 6: Full Layout (Bottom Layers)

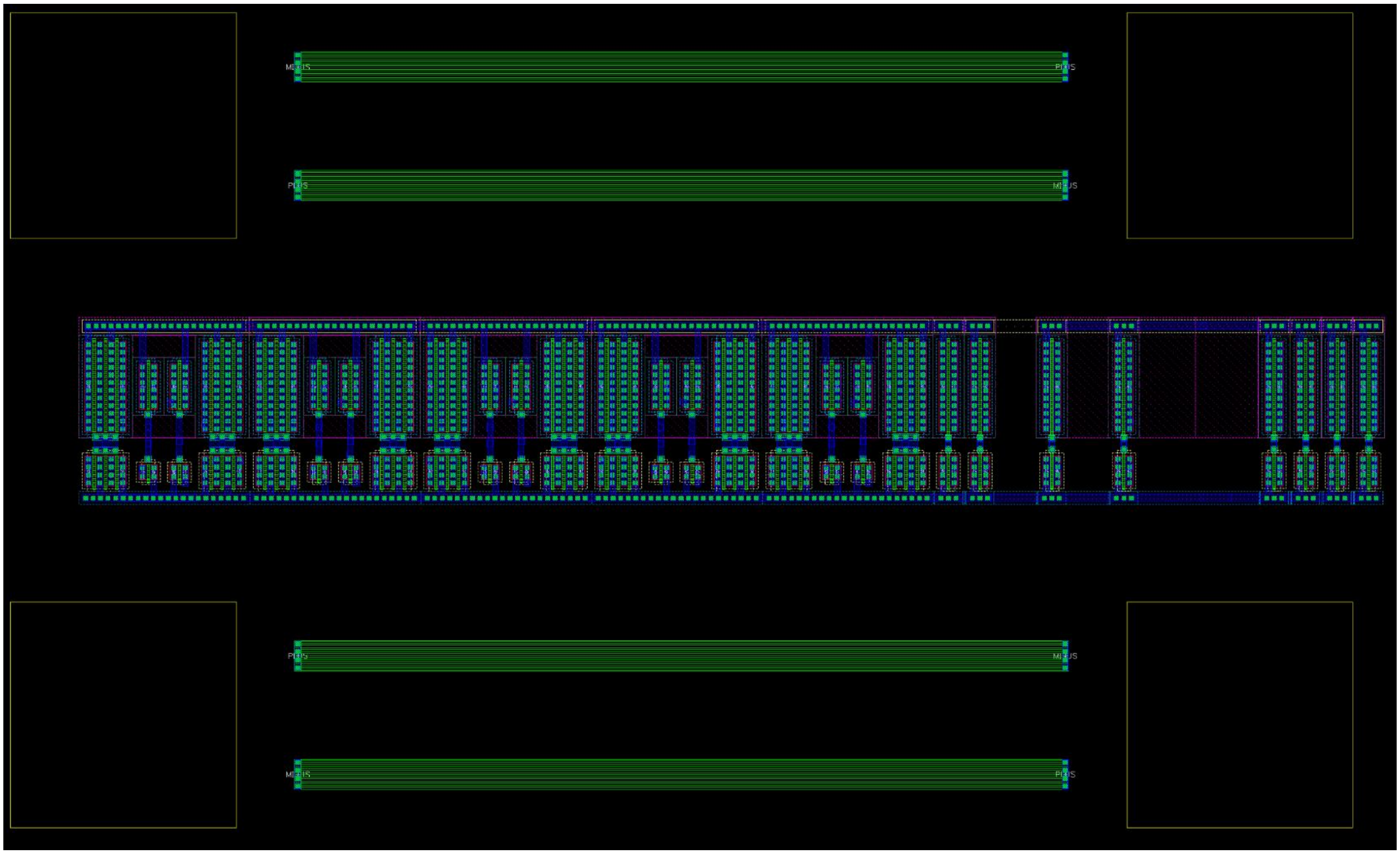


Figure 7: Full Layout through m1

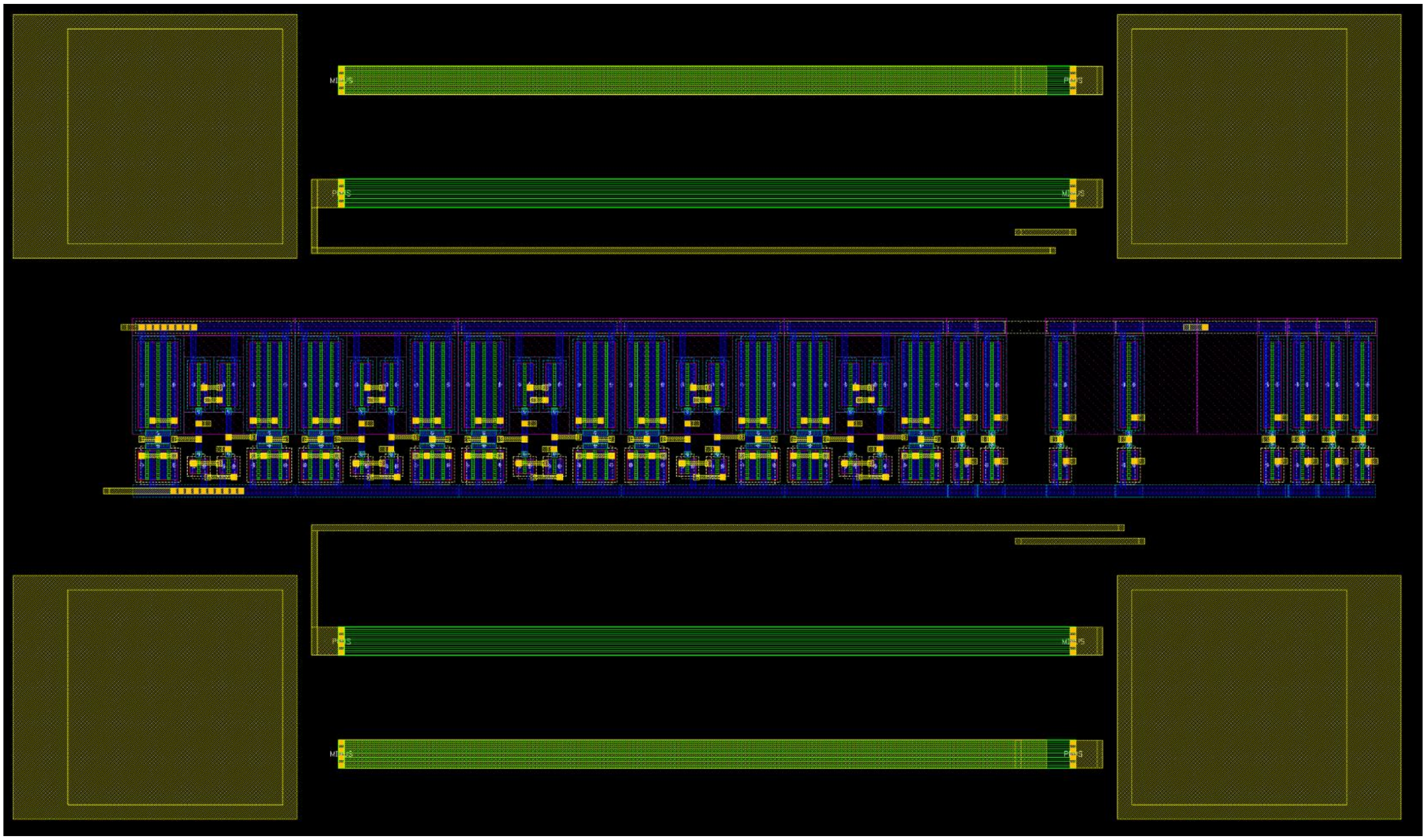


Figure 8: Full Layout through m2

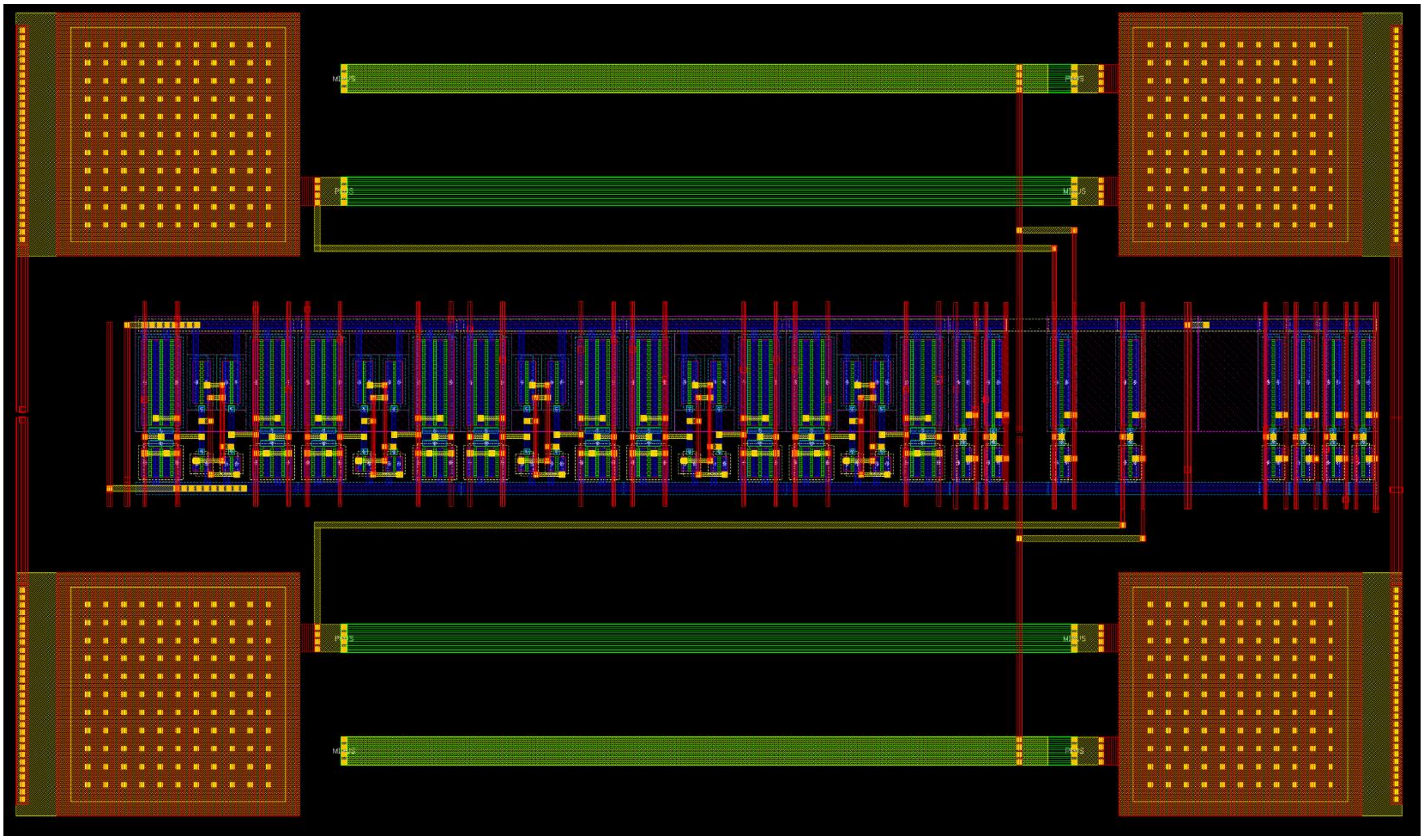


Figure 9: Full Layout through m3

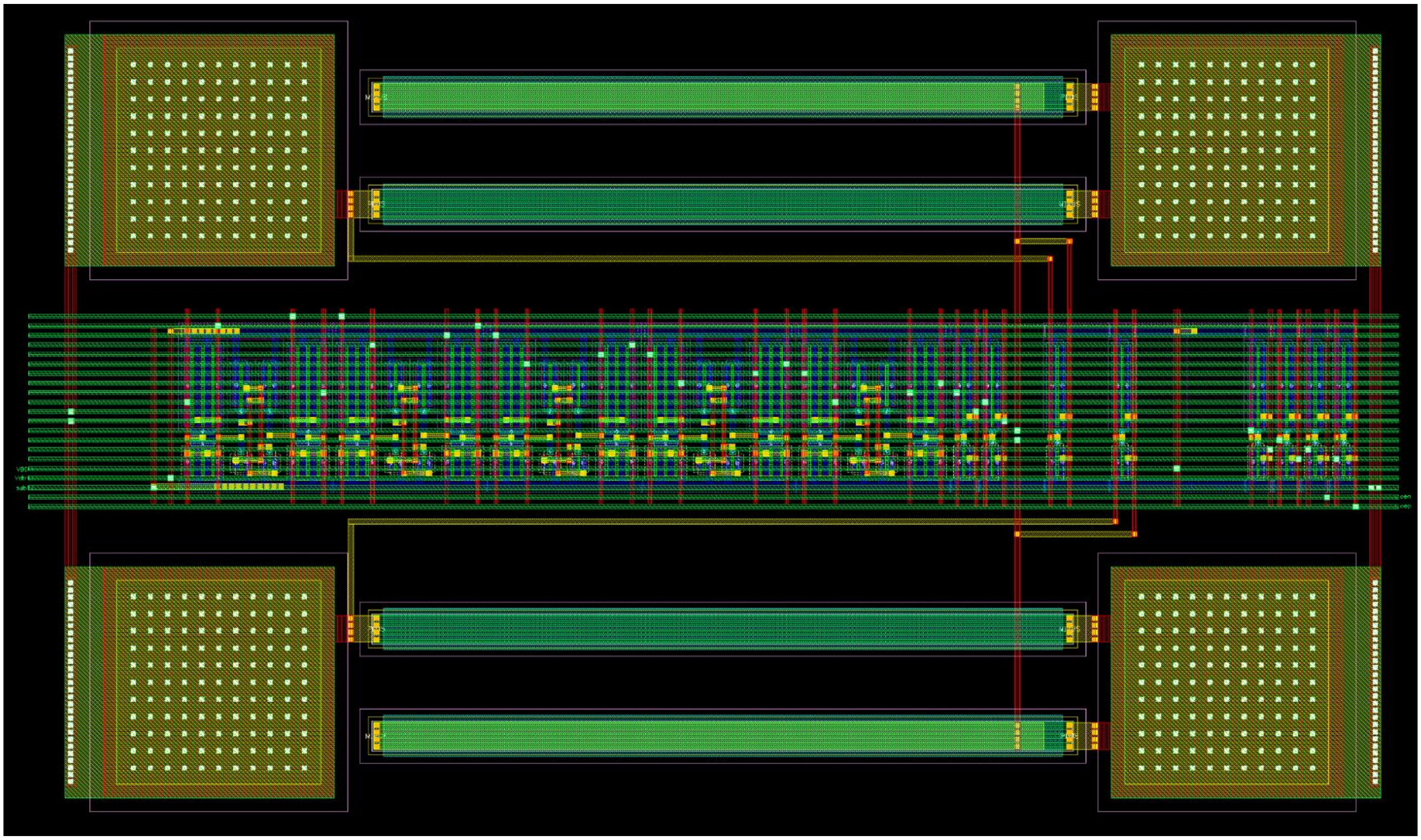


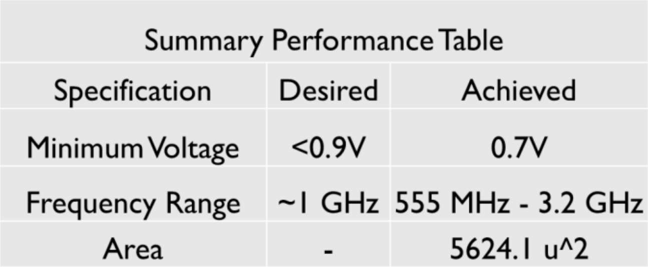
Figure 10: Full Layout

VII. CHALLENGES

This project introduced me to a wide variety of challenges, especially with the layout portion of the design. Being the largest layout I had ever done, I found it very easy to get lost or lose my place when routing long signals across the full width. I was able to partially compensate for this by using the layer menu often, but in future designs I will probably make use of a tool like LayoutXL to assist with routing the traces. Additionally, I spent a lot of time figuring out the ac-coupling circuitry, as I was unfamiliar with how to properly accomplish the common mode problem. I also had a very hard time getting a clean LVS, which eventually turned out to be an issue with the substrate tie on the resistor and capacitor which was labeled “sub!”. After eventually figuring this out, I renamed VSS in my top-level design in both the layout and schematic to “sub!” and had a clean LVS. It was also challenging to achieve symmetry with such a large design. Thankfully, symmetry wasn’t of utmost importance in this particular design, but I have found symmetry to be hard to achieve in general as designs become larger. Overall, I found this design to be particularly challenging in the layout but was able to find solutions and was able to pass both DRC and LVS. I was largely unfamiliar with VCOs before this project, so it was instructional both in terms of the circuit design aspect as well as the layout aspect.

VIII. RESULTS

Figure 11 shows the functionality of the voltage-controlled oscillator using a simple testbench in Virtuoso. The input control voltage is ramped down from the power supply and the output can be seen oscillating, with the frequency linearly decreasing. With this testbench, the input control voltage range was determined to be 1.1V, and the output frequency range was found to be 2.65 GHz.



Summary Performance Table

Specification	Desired	Achieved
Minimum Voltage	<0.9V	0.7V
Frequency Range	~1 GHz	555 MHz - 3.2 GHz
Area	-	5624.1 u^2

IX. CONCLUSION

A relaxation VCO has been presented that uses a relatively simple topology but accomplishes an important function. Voltage controlled oscillators with high signal purity provide the foundation for systems like phase locked loops which are often used in on-chip clock generators. This project has been very instructional in learning the basics of voltage controlled oscillators, and especially layout techniques for larger layouts. Large layouts in particular can be extremely difficult to debug if not done methodically, and routing traces can be very tedious without the use of a tool like LayoutXL. One big time saver in this project was designing the smaller cells in such a way that integration with the larger system was seamless, particularly the height of the cells. In addition, testing

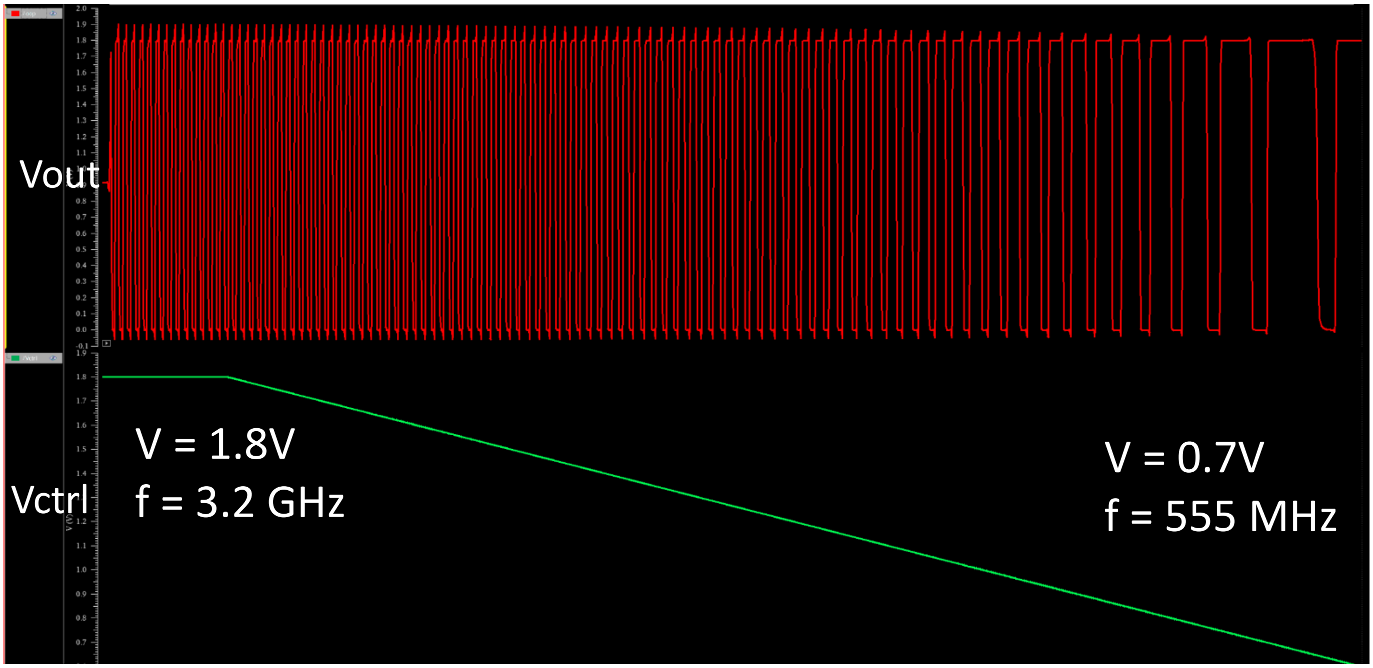


Figure 11: VCO Functionality

the functionality of new components like the poly resistors and MIM capacitors in a small testbench was helpful. Attempting to integrate such components into the entire layout from the beginning is unlikely to pass DRC/LVS and understanding how the node connections are made is critical. Through this technique was how the “VSS/sub!” issue was discovered and remedied. Overall, there are no real shortcuts in layout. Practice and learning special techniques definitely speed the overall process along but being sloppy or rushing through the early stages will ultimately waste time in the long run. Overall, the VCO presented in this project is a functional circuit block and was challenging yet satisfying to design.

XVI. References

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[3] W. J. Dally and J. W. Poulton, *Digital Systems Engineering*. Cambridge: Cambridge University Press, 2008.